

FIG. 1 PRIOR ART

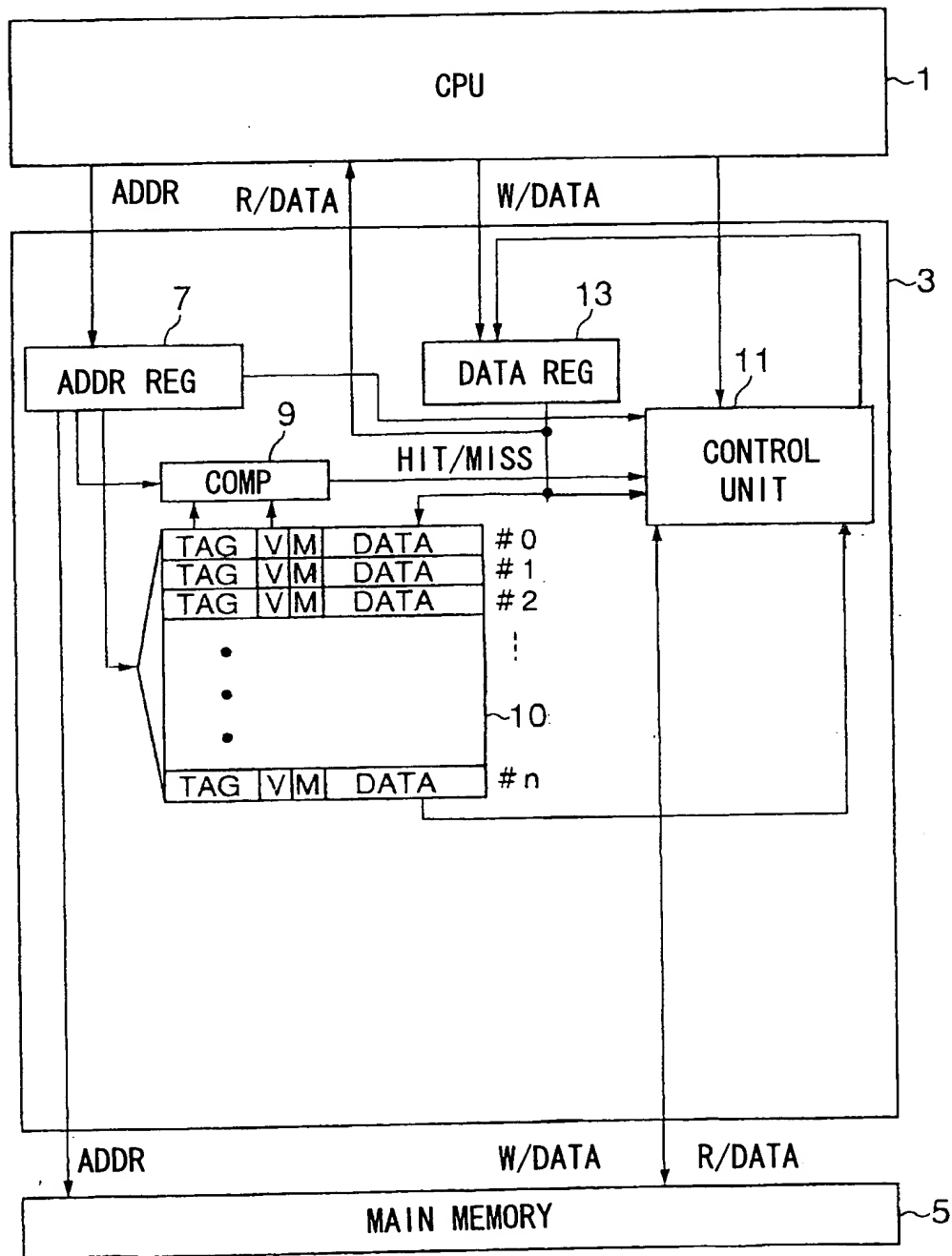


FIG. 2 PRIOR ART

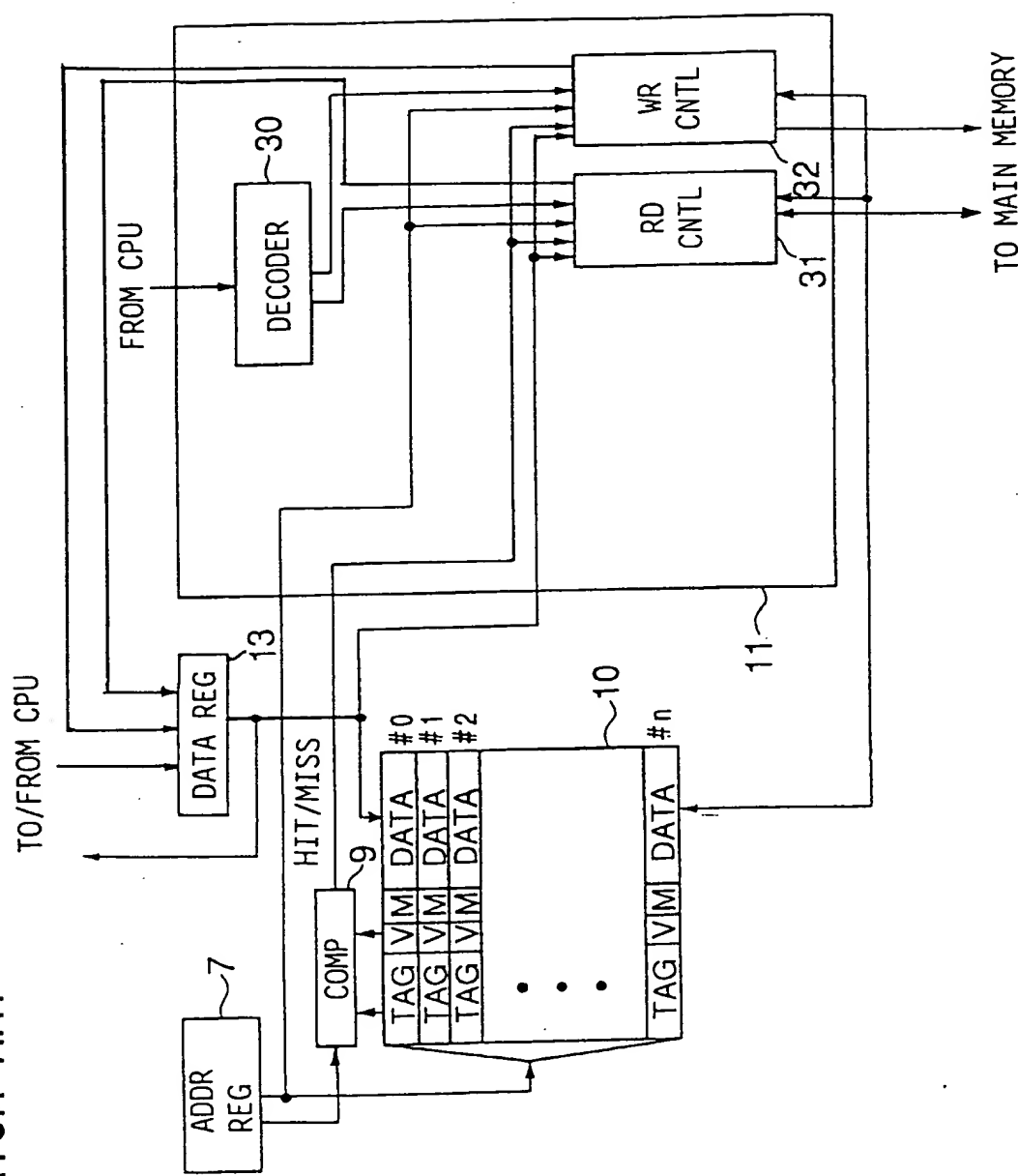


FIG. 3 PRIOR ART

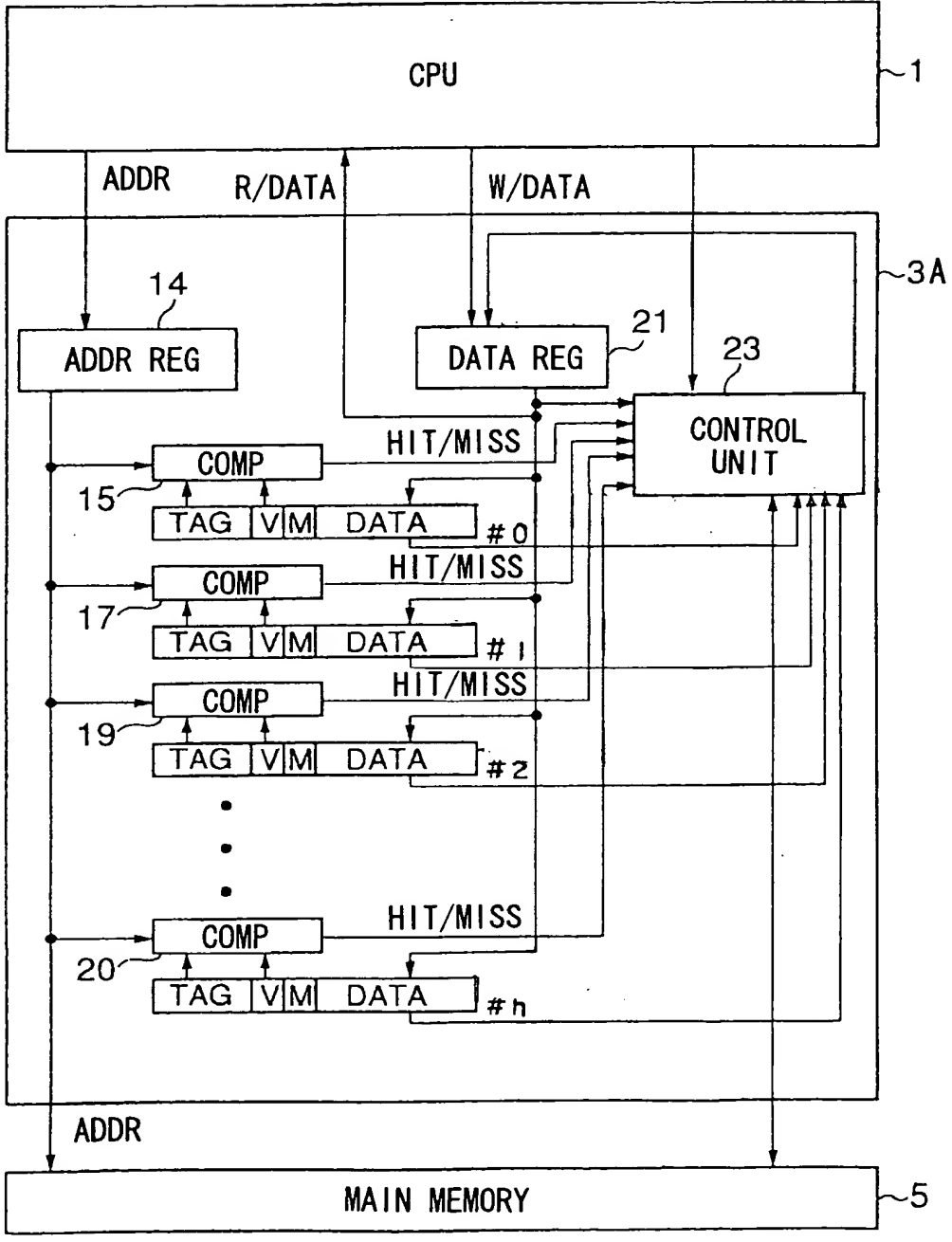


FIG. 4 PRIOR ART

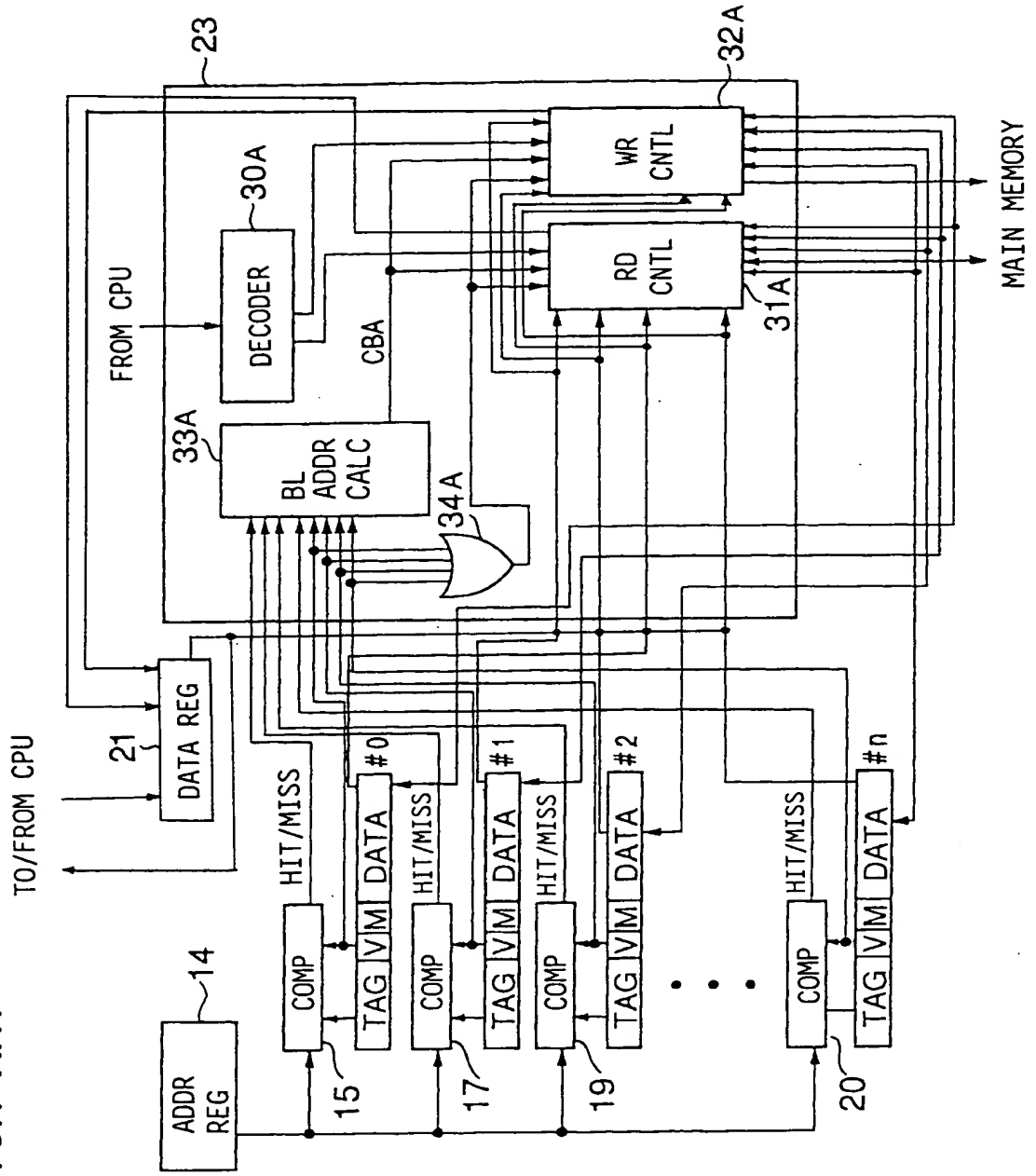


FIG. 5 PRIOR ART

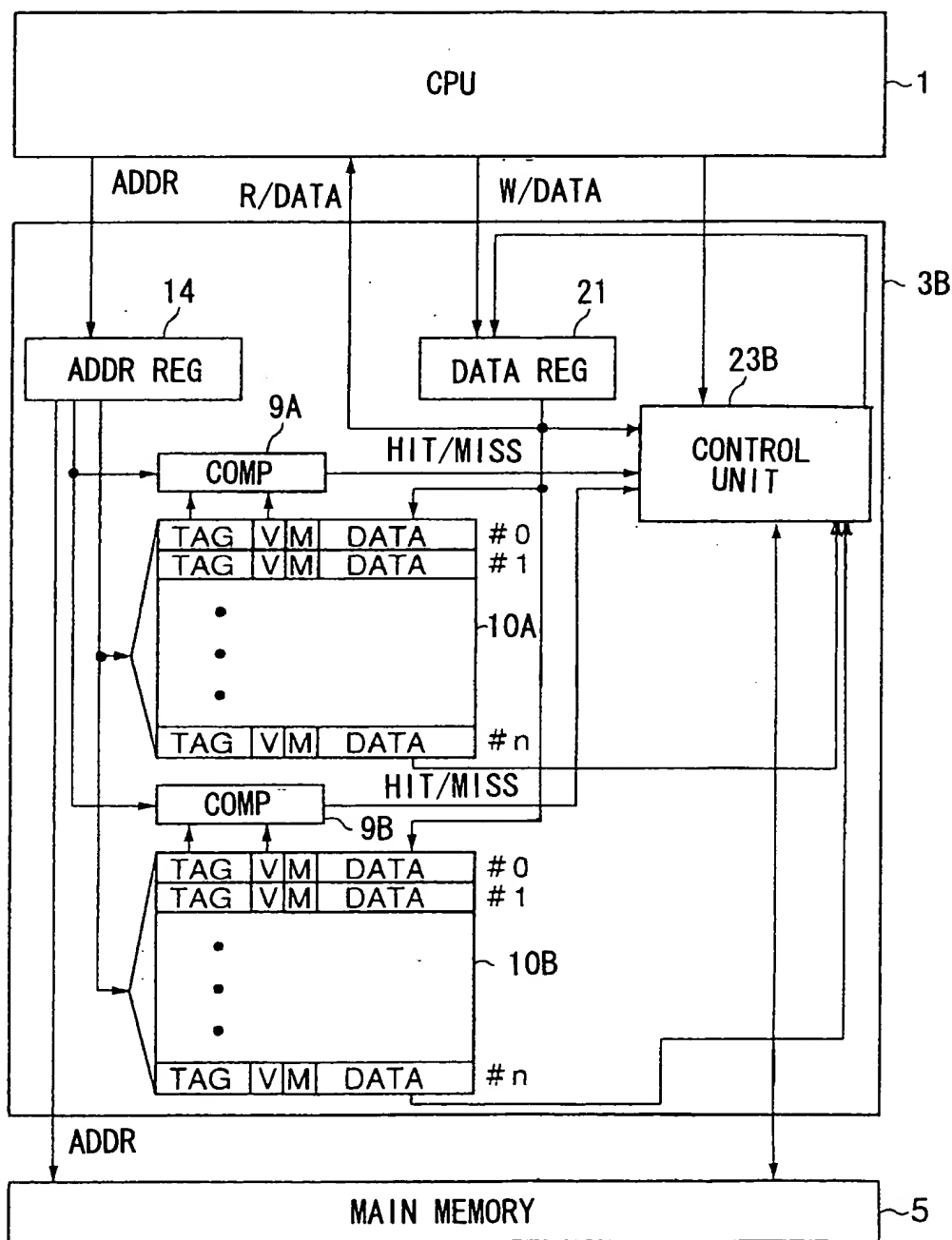


FIG. 6 PRIOR ART

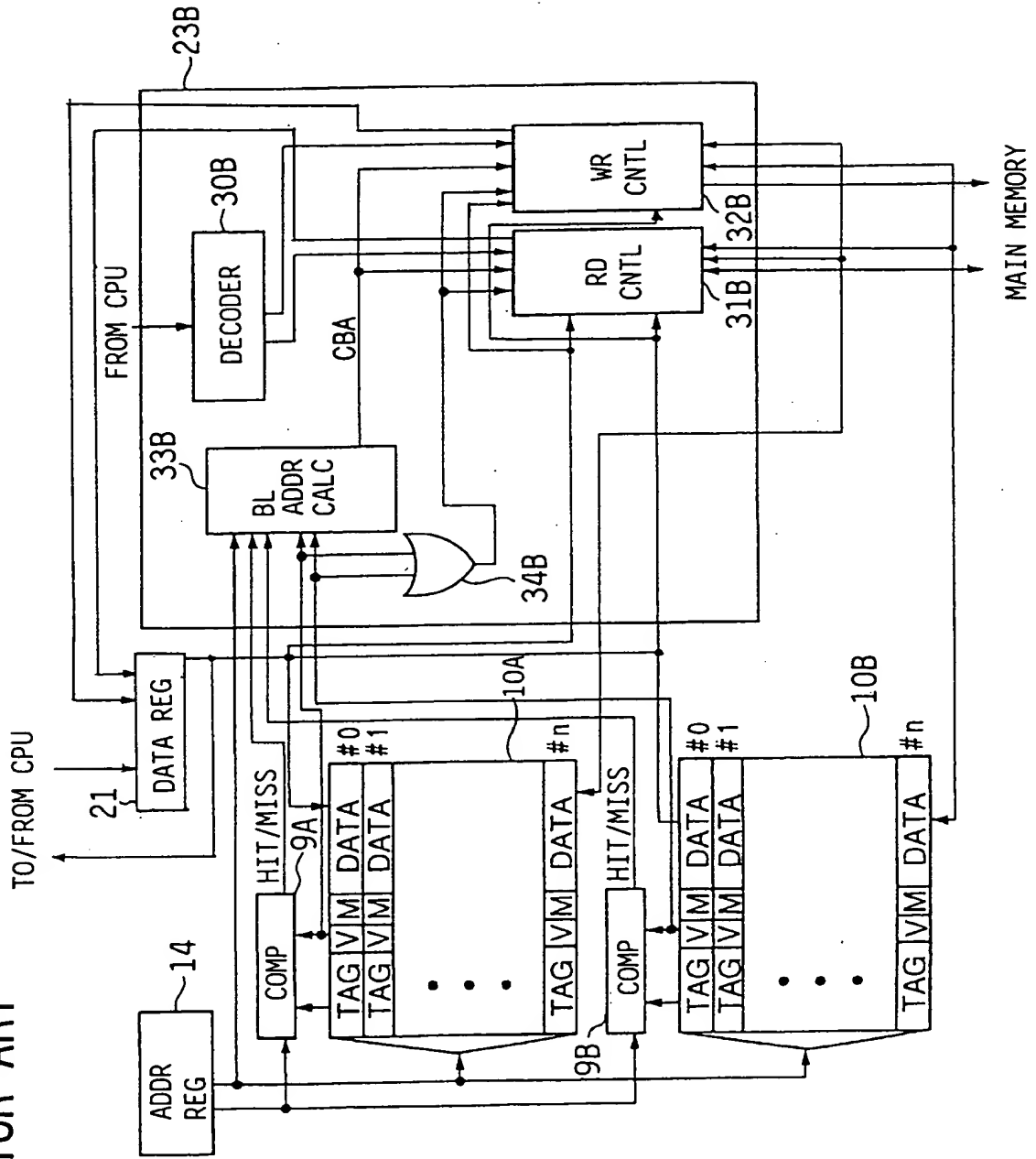


FIG. 7

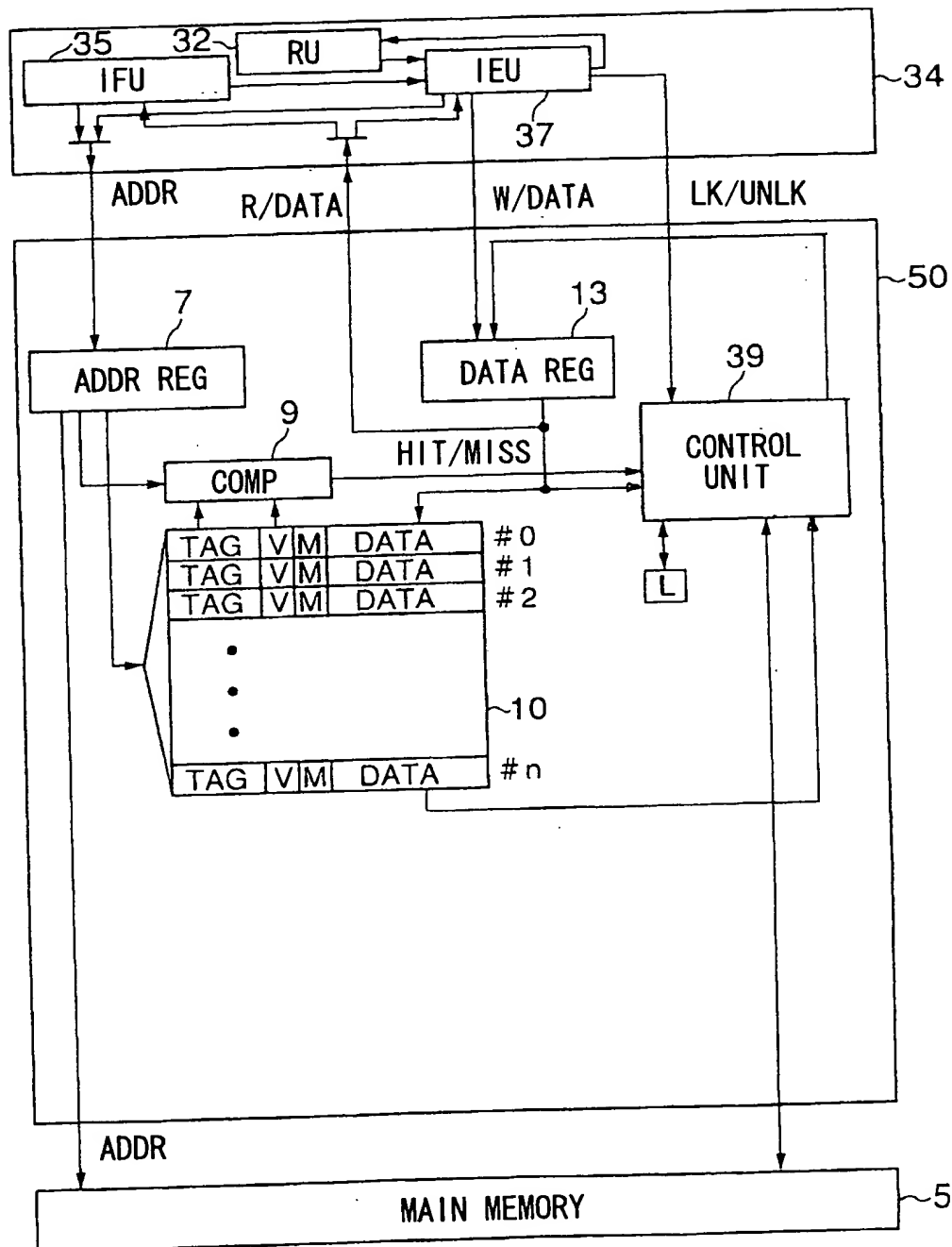


FIG. 8

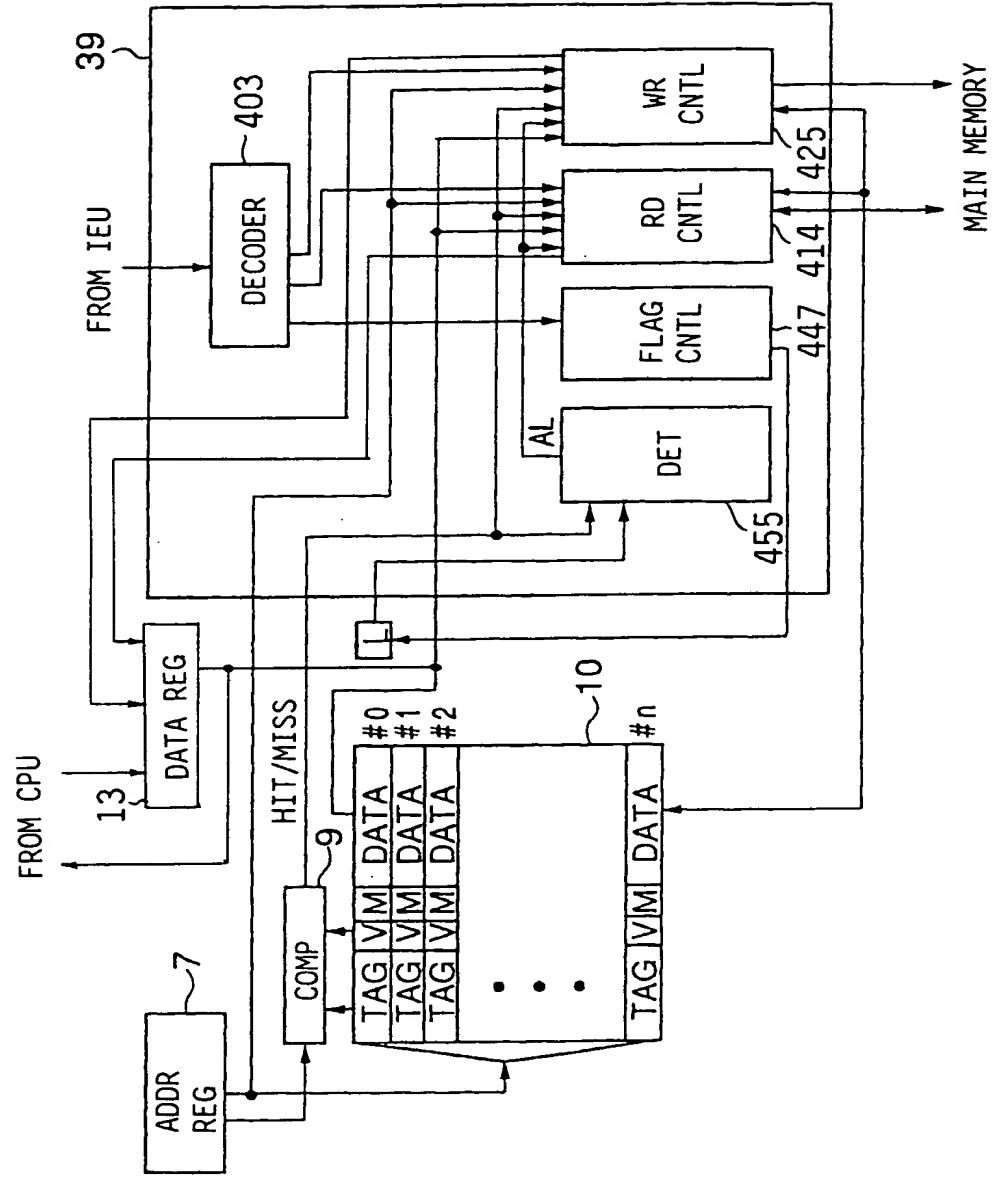


FIG. 9

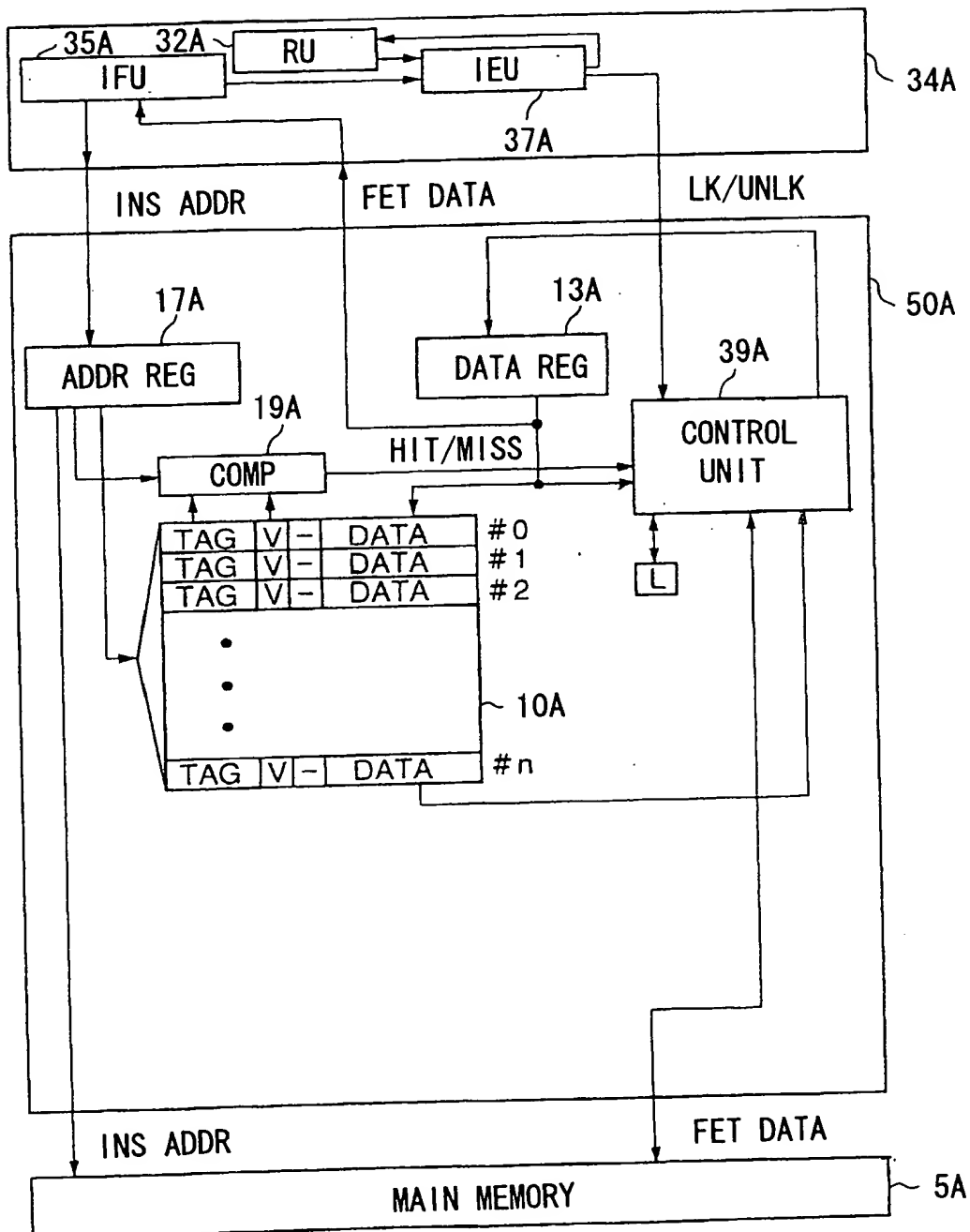


FIG. 10

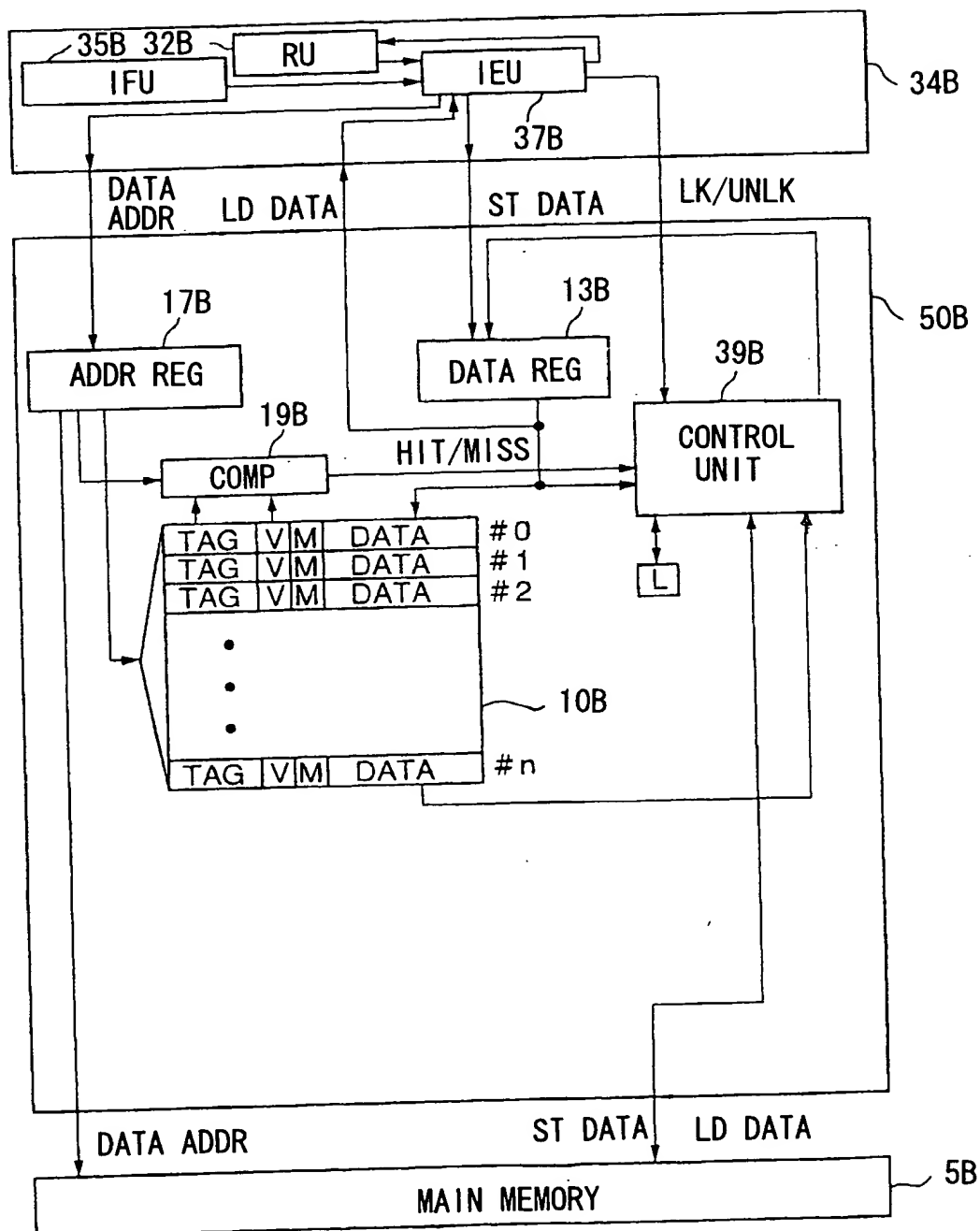


FIG. 12

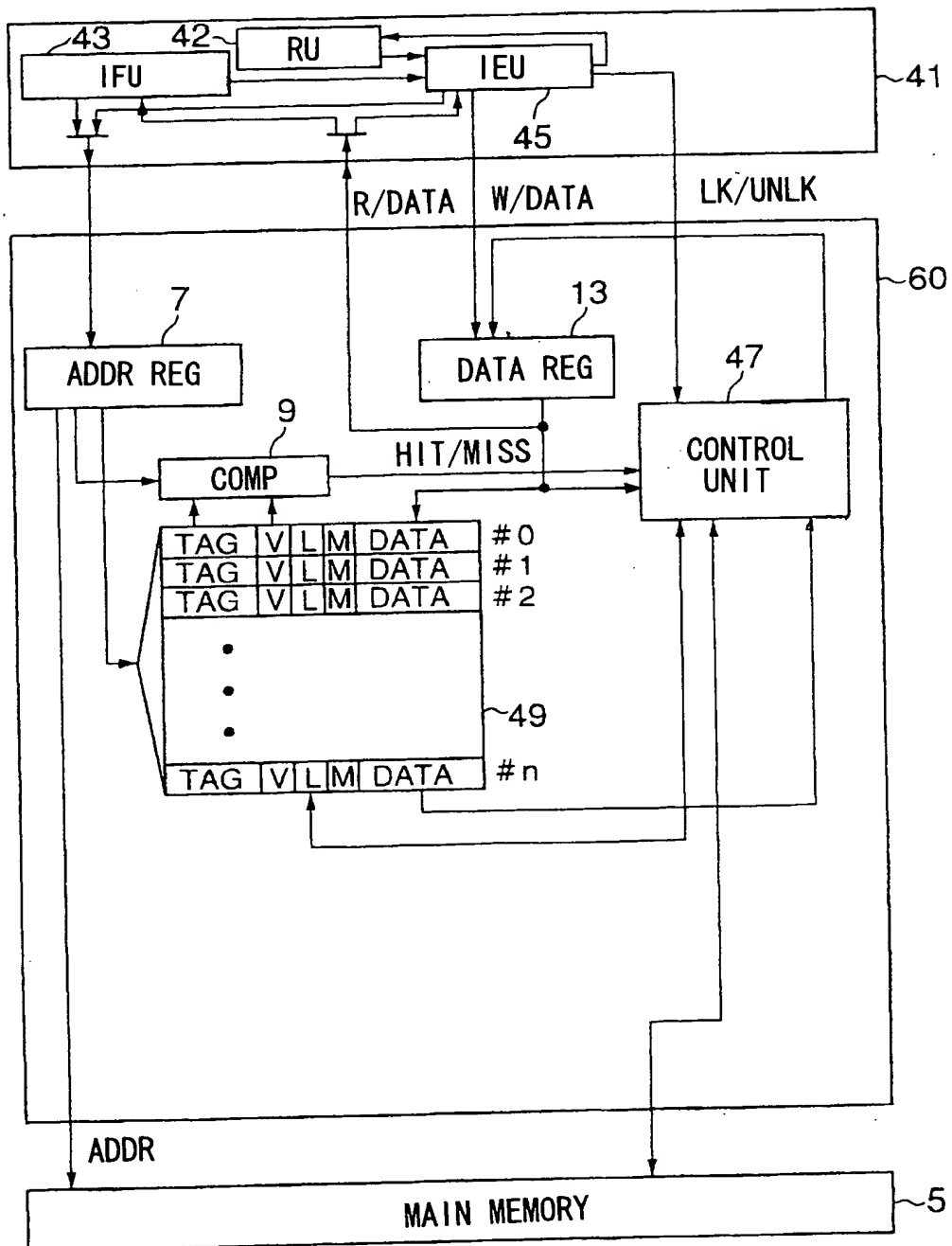
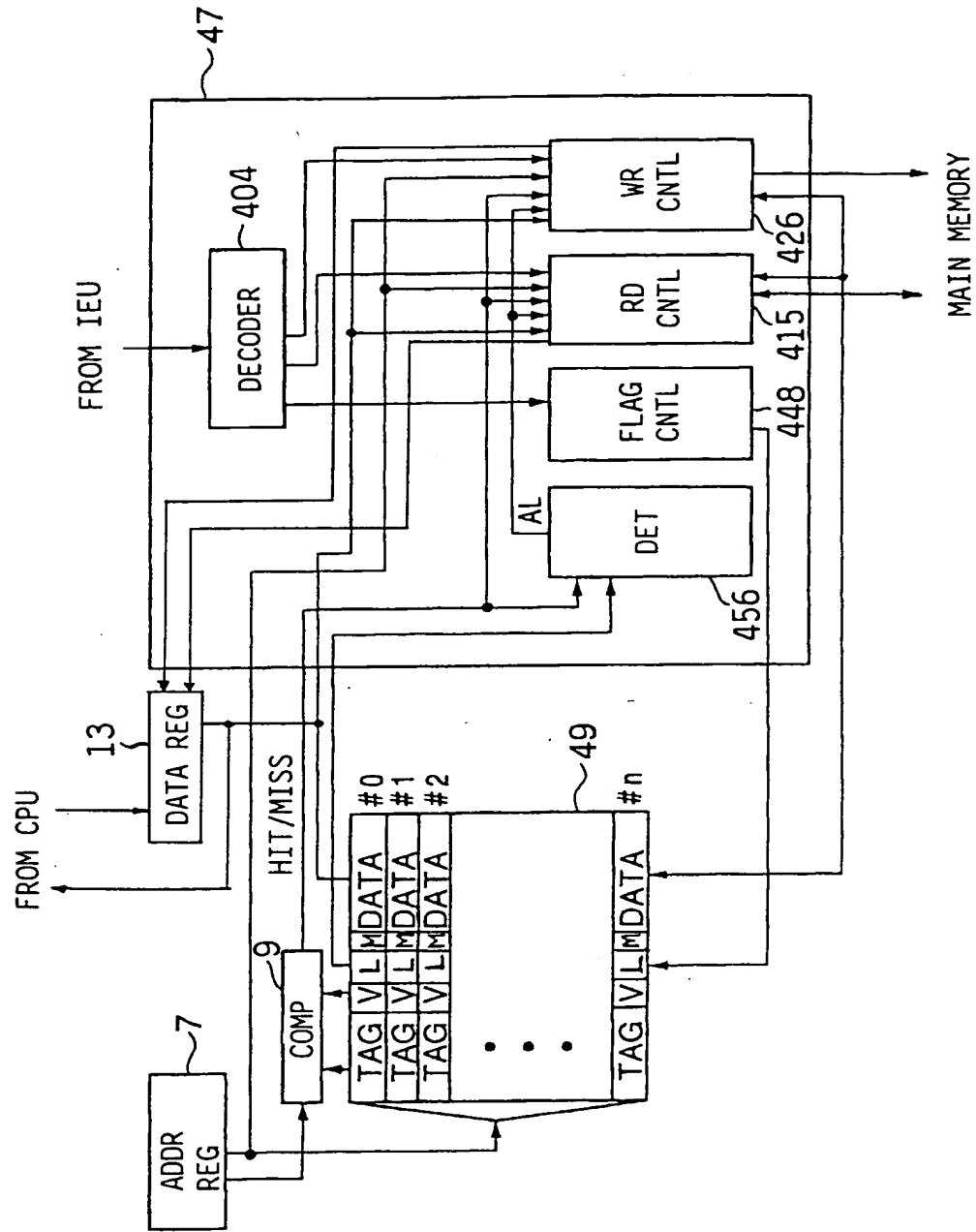


FIG. 13



APPROVED	O.G. FIG.	
EBY	DATE	BY
12/17/2000		

FIG. 14

OP-CODE	BASE	OFFSET
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FIG. 15

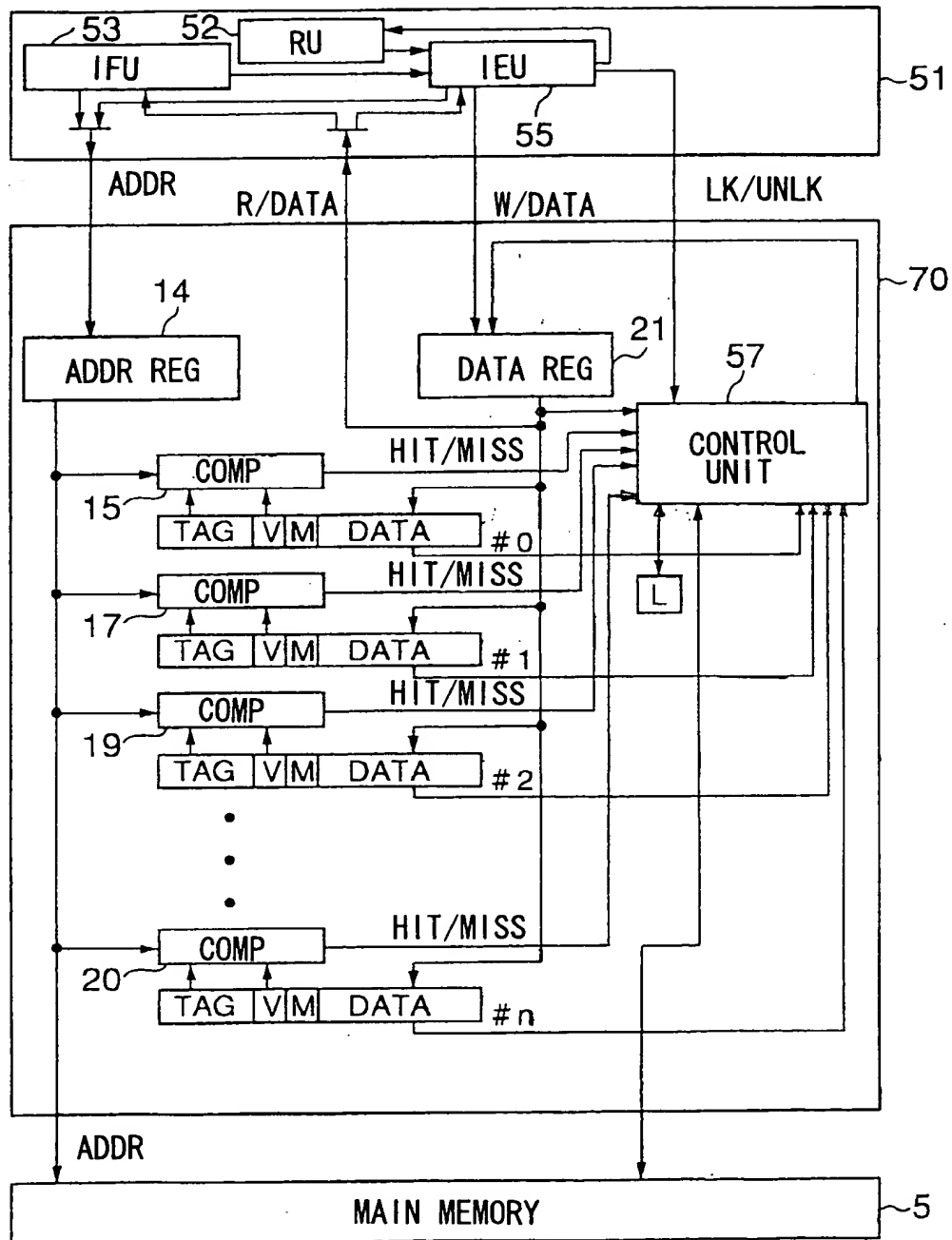


FIG. 16

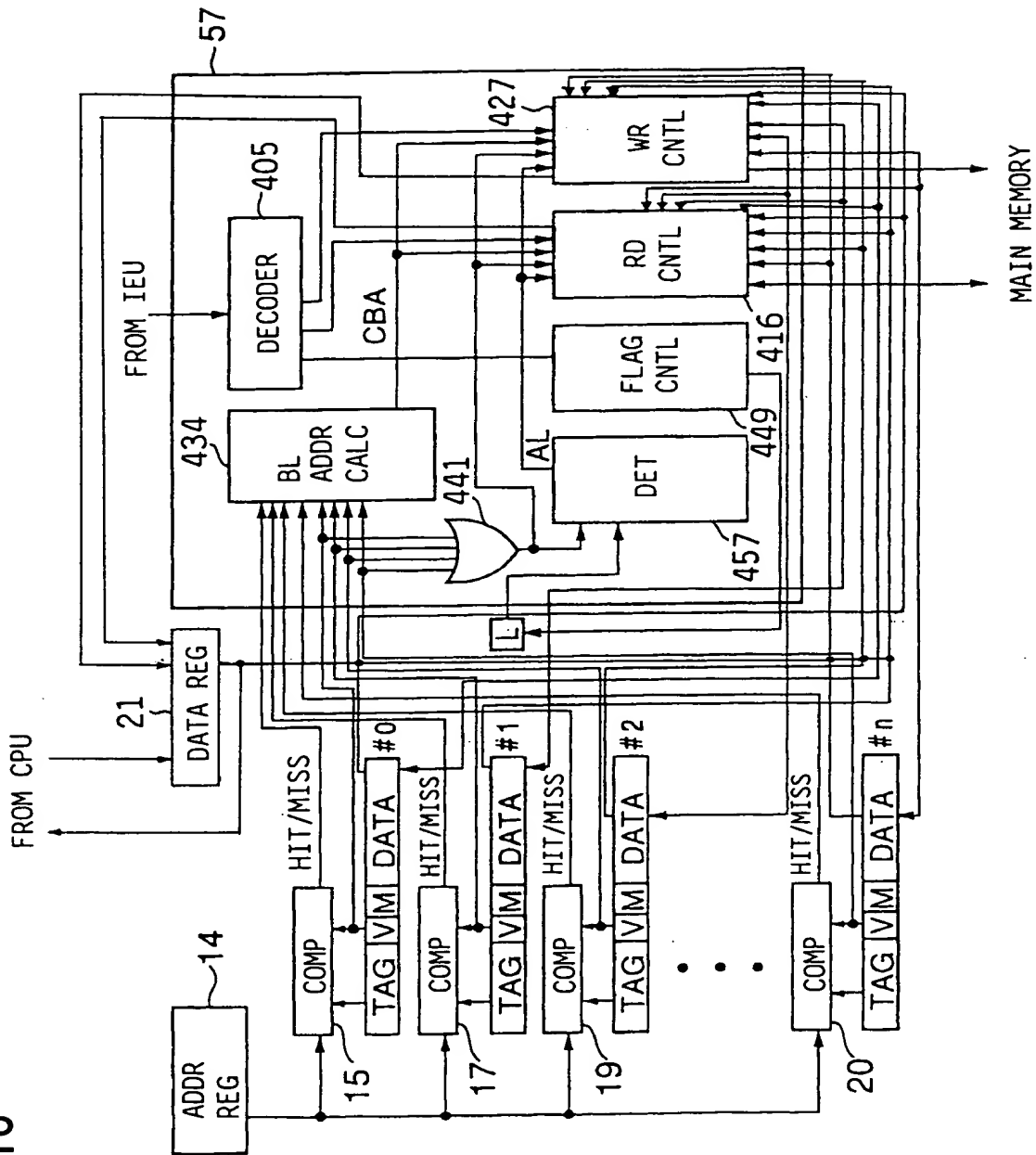


FIG. 17

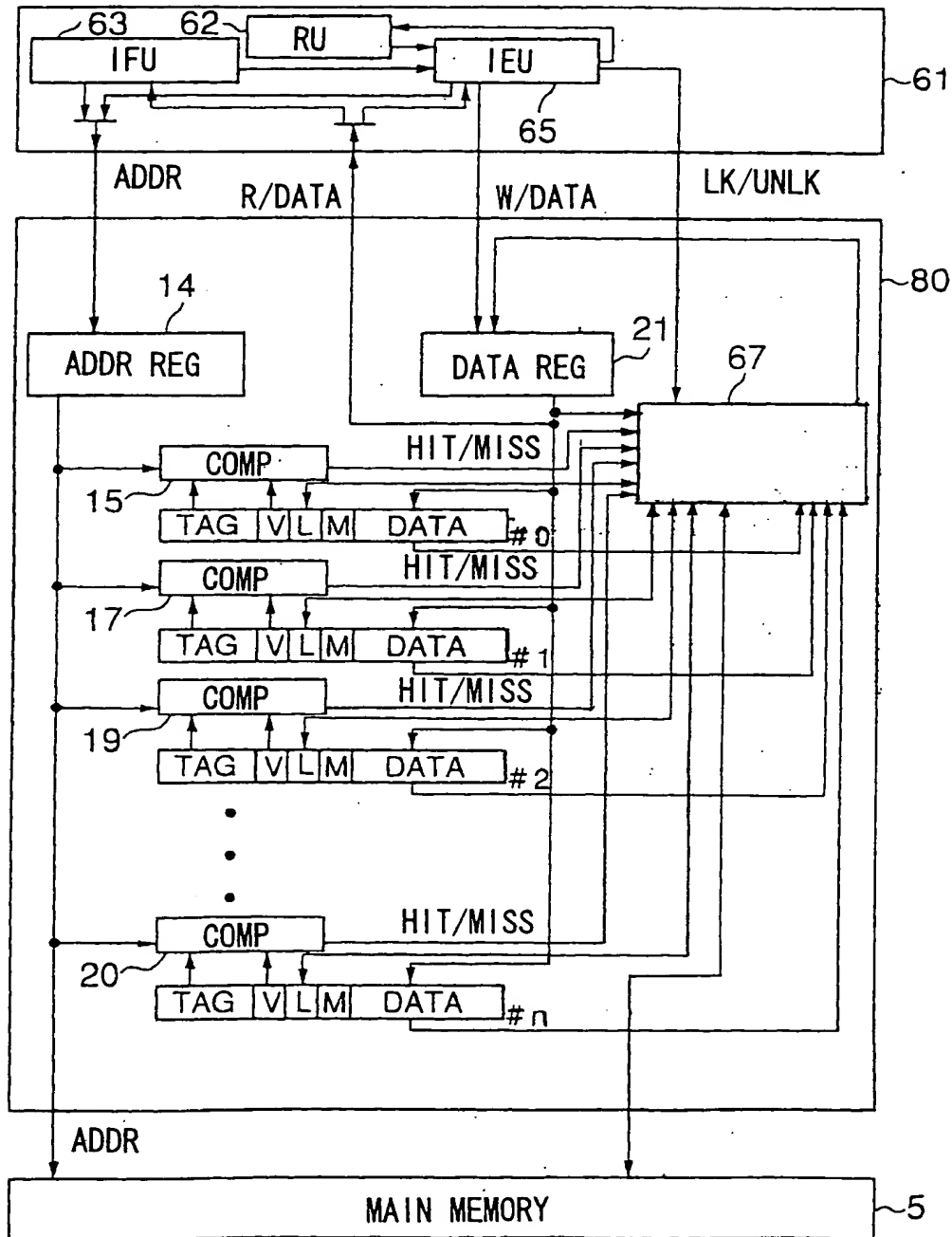
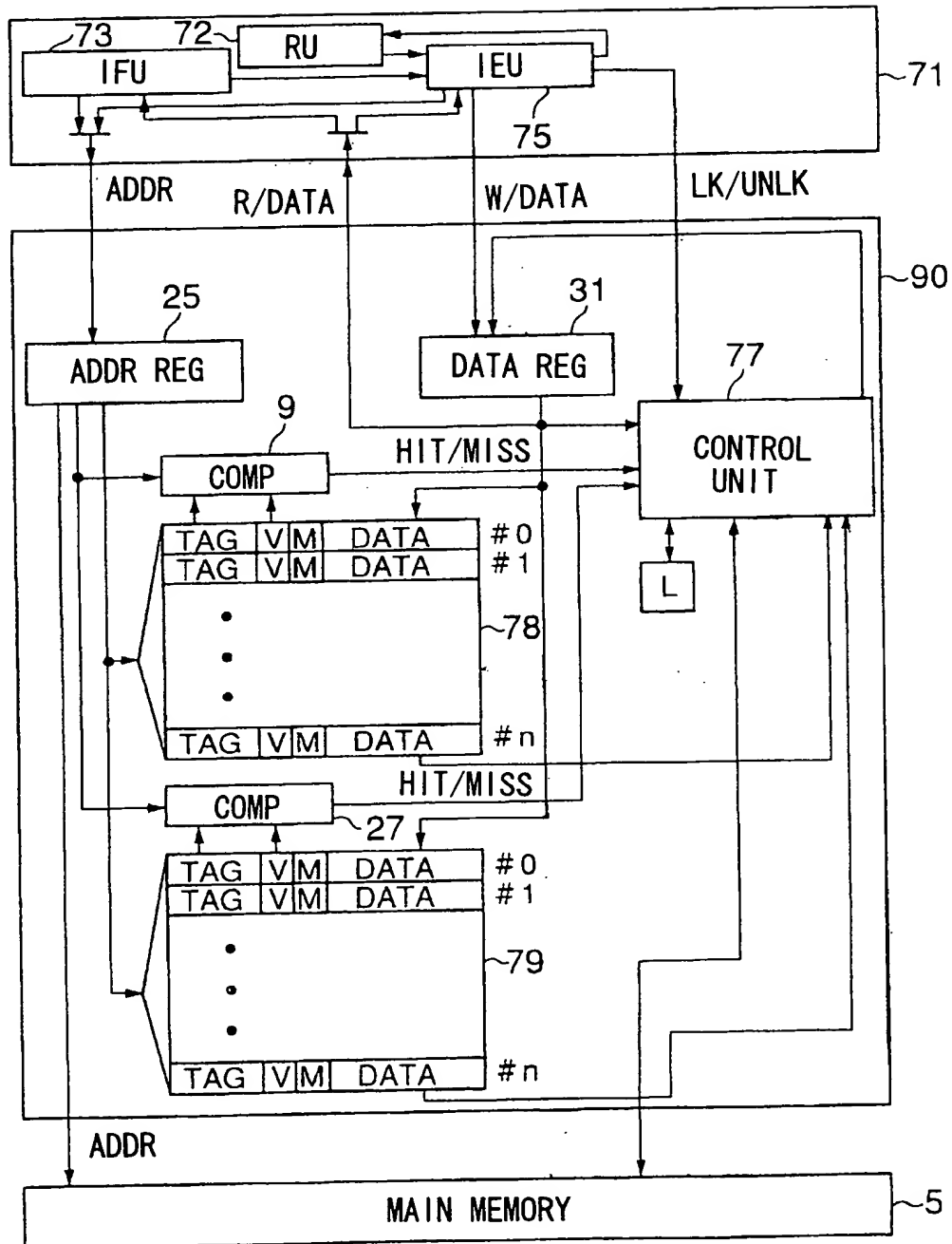


FIG. 19



The diagram illustrates the internal components and data flow of a cache system. On the left, the 'FROM CPU' interface includes an 'ADDR REG' (25) and a 'DATA REG' (31). The 'ADDR REG' (25) provides an address to a 'COMP' (27) and an 'ADDR REG' (25). The 'DATA REG' (31) provides data to a 'COMP' (27) and an 'ADDR REG' (25). The 'COMP' (27) outputs a 'HIT/MISS' signal (9) to the cache. The cache (78) consists of multiple entries, each with a 'TAG' and 'DATA' field. The 'HIT/MISS' signal (9) is used to control the cache. The cache (78) is connected to a 'BL ADDR CALC' (436) and a 'DET' (451). The 'BL ADDR CALC' (436) outputs a 'CBA' (443) signal to the 'DET' (451). The 'DET' (451) outputs a 'L' (459) signal to the 'DATA REG' (31). The 'DATA REG' (31) also outputs a 'FROM IEU' signal (77) to the 'DECODE' (407). The 'DECODE' (407) outputs control signals to the 'WR CNTL' (429), 'RD CNTL' (418), and 'FLAG CNTL' (451). The 'WR CNTL' (429), 'RD CNTL' (418), and 'FLAG CNTL' (451) are connected to the 'MAIN MEMORY' on the right. The 'MAIN MEMORY' outputs data to the 'DATA REG' (31) and the 'FROM CPU' interface.

FIG. 21

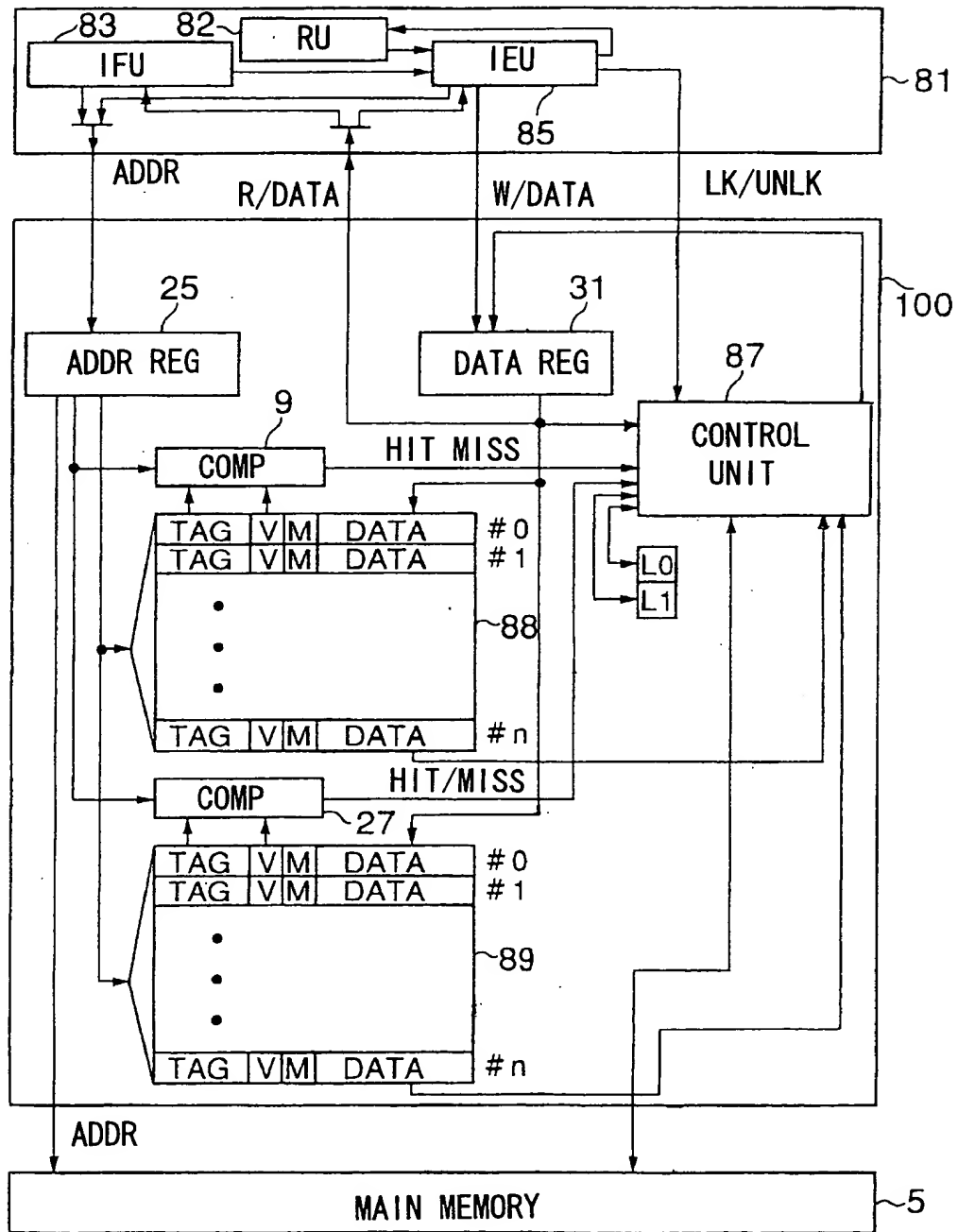
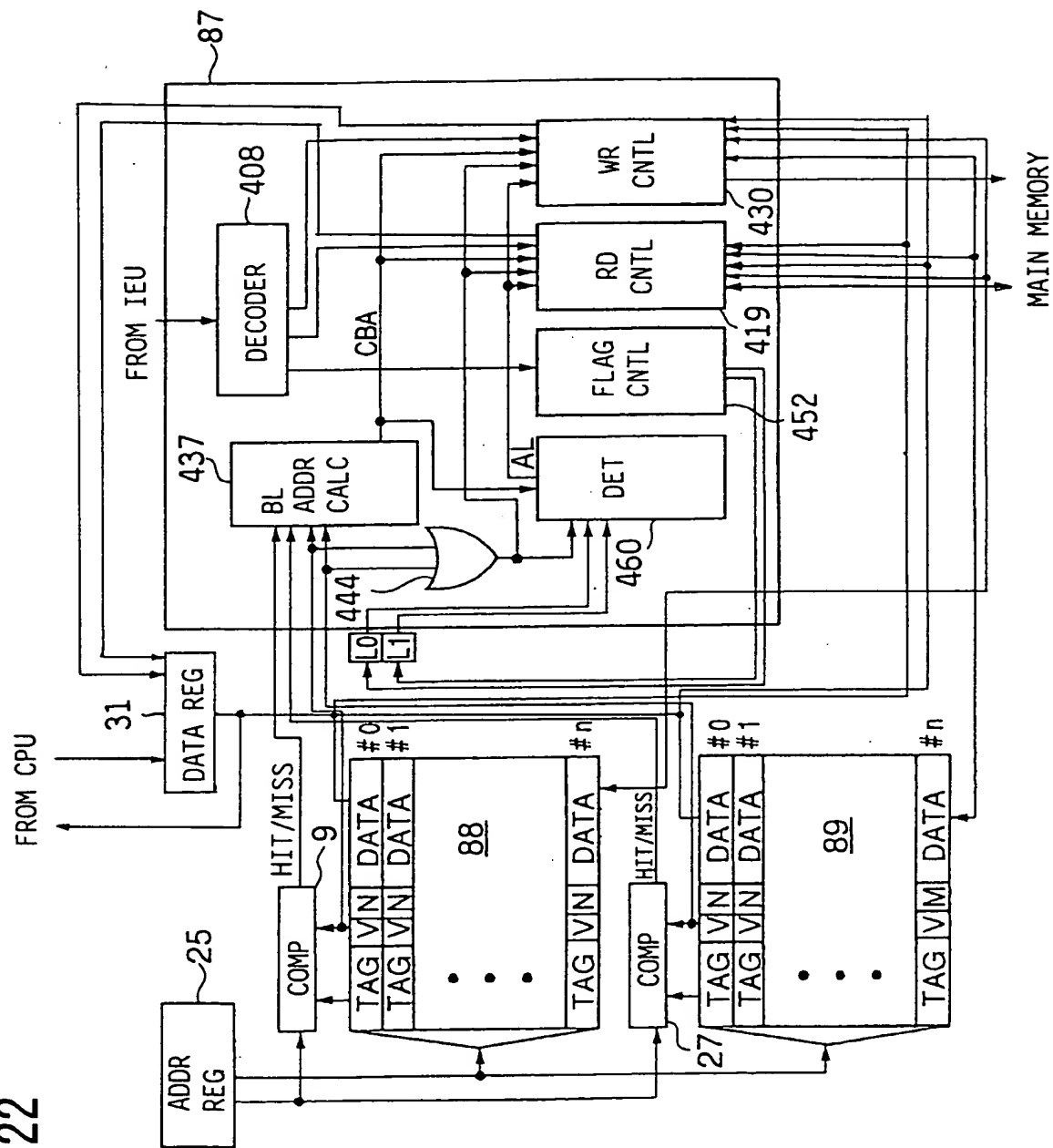


FIG. 22



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		
	147AF	

FIG. 23

OP-CODE	—	WAY
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FIG. 24

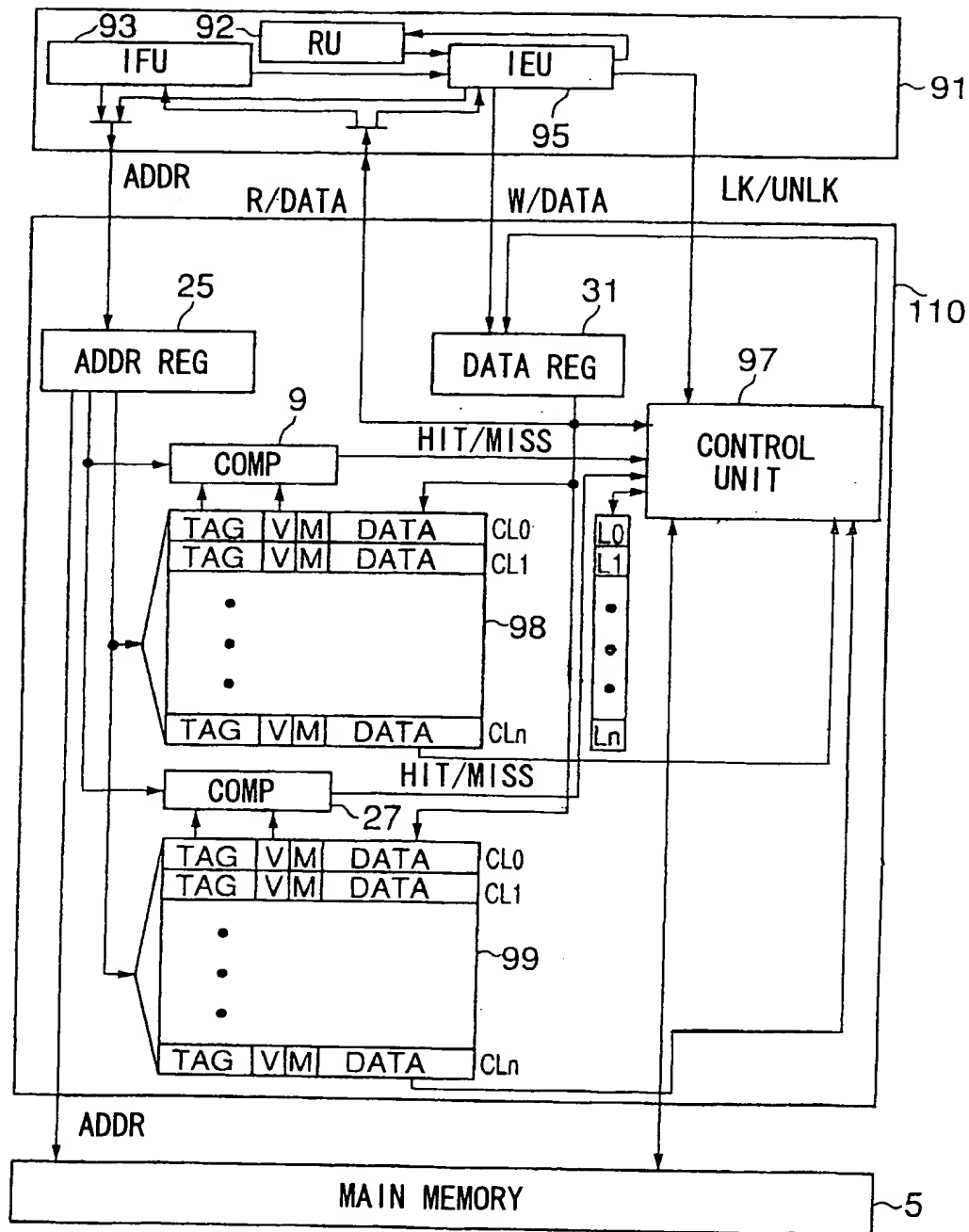
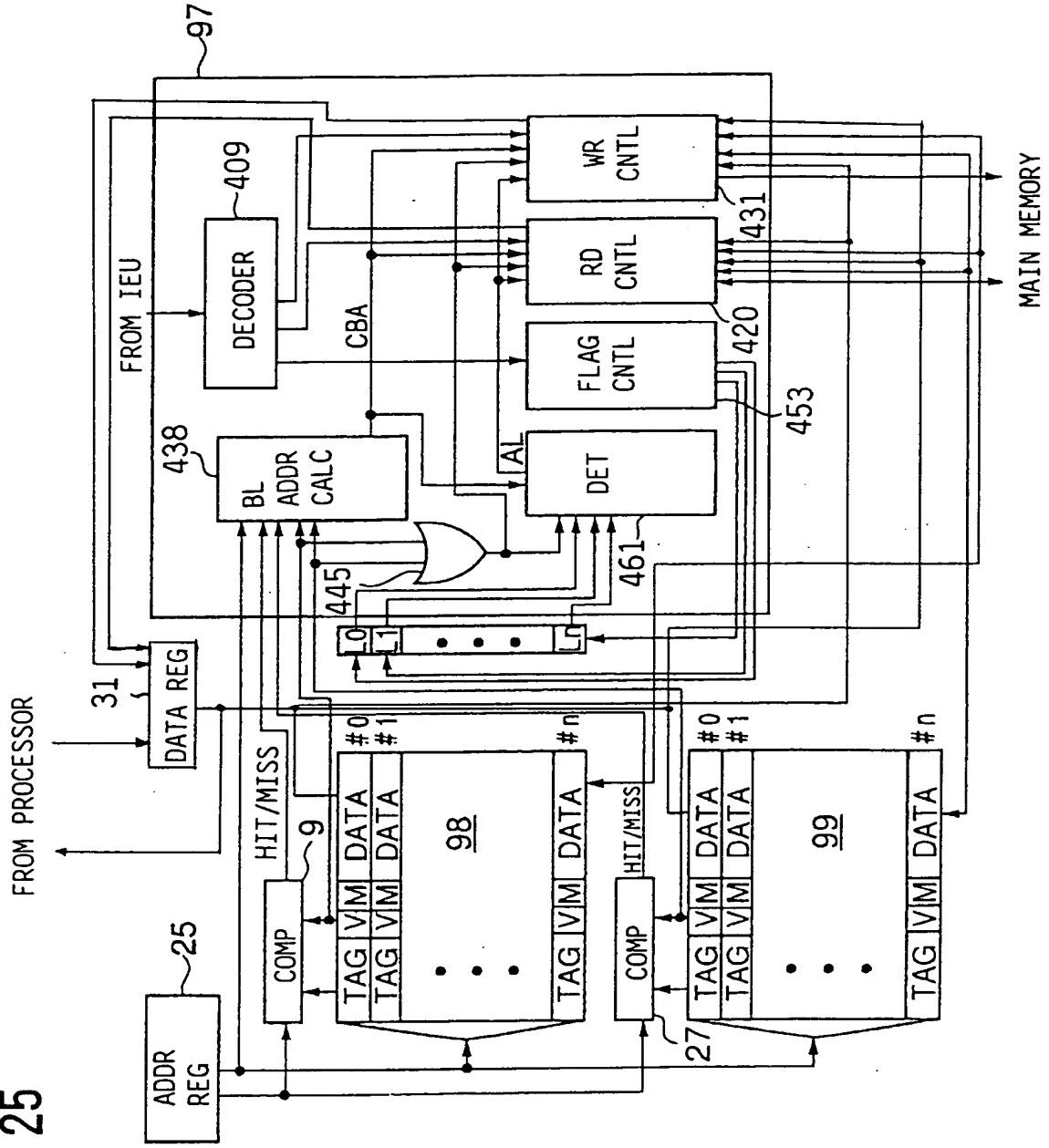


FIG. 25



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FIG. 26

OP-CODE	—	LINE
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FIG. 27

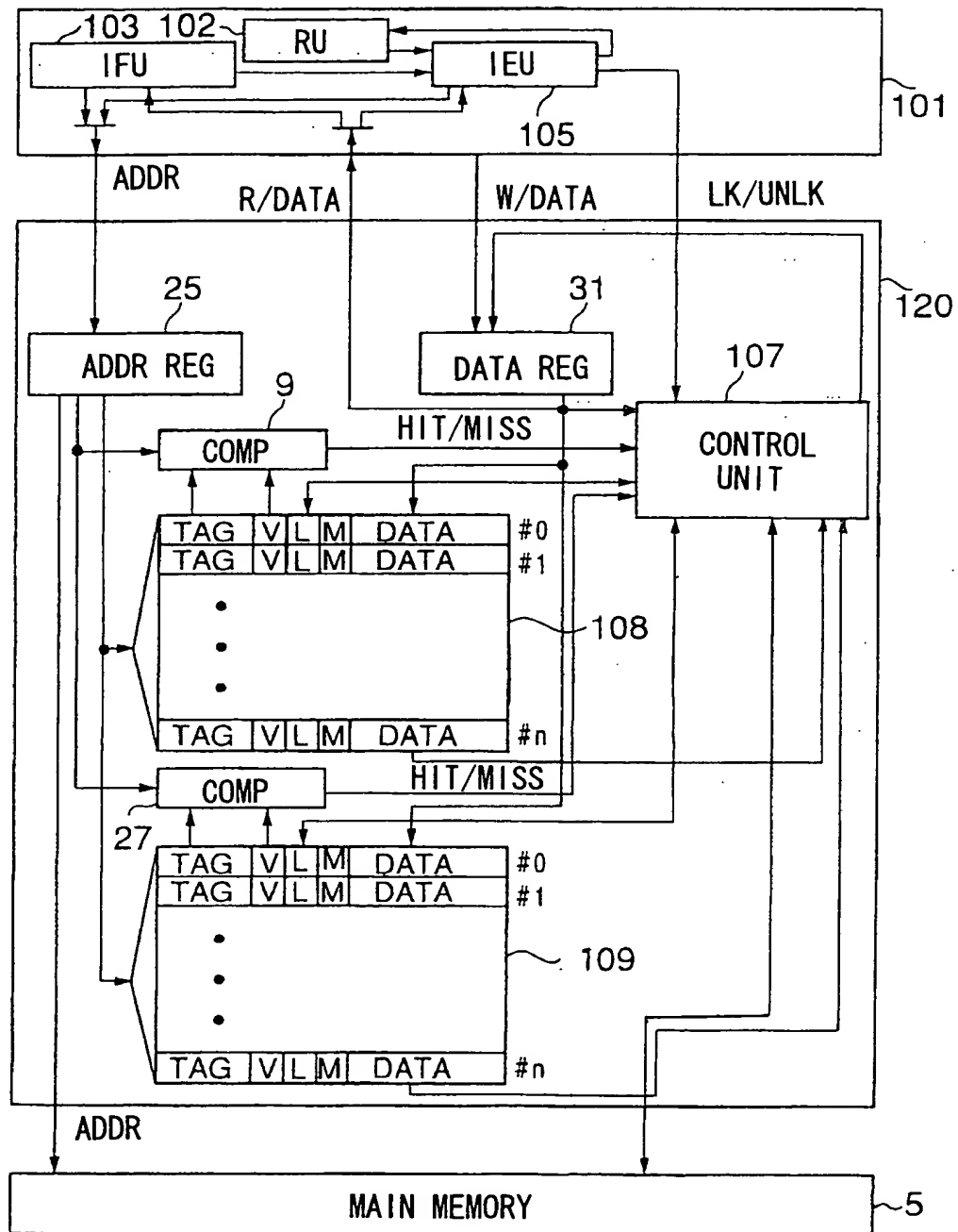


FIG. 28

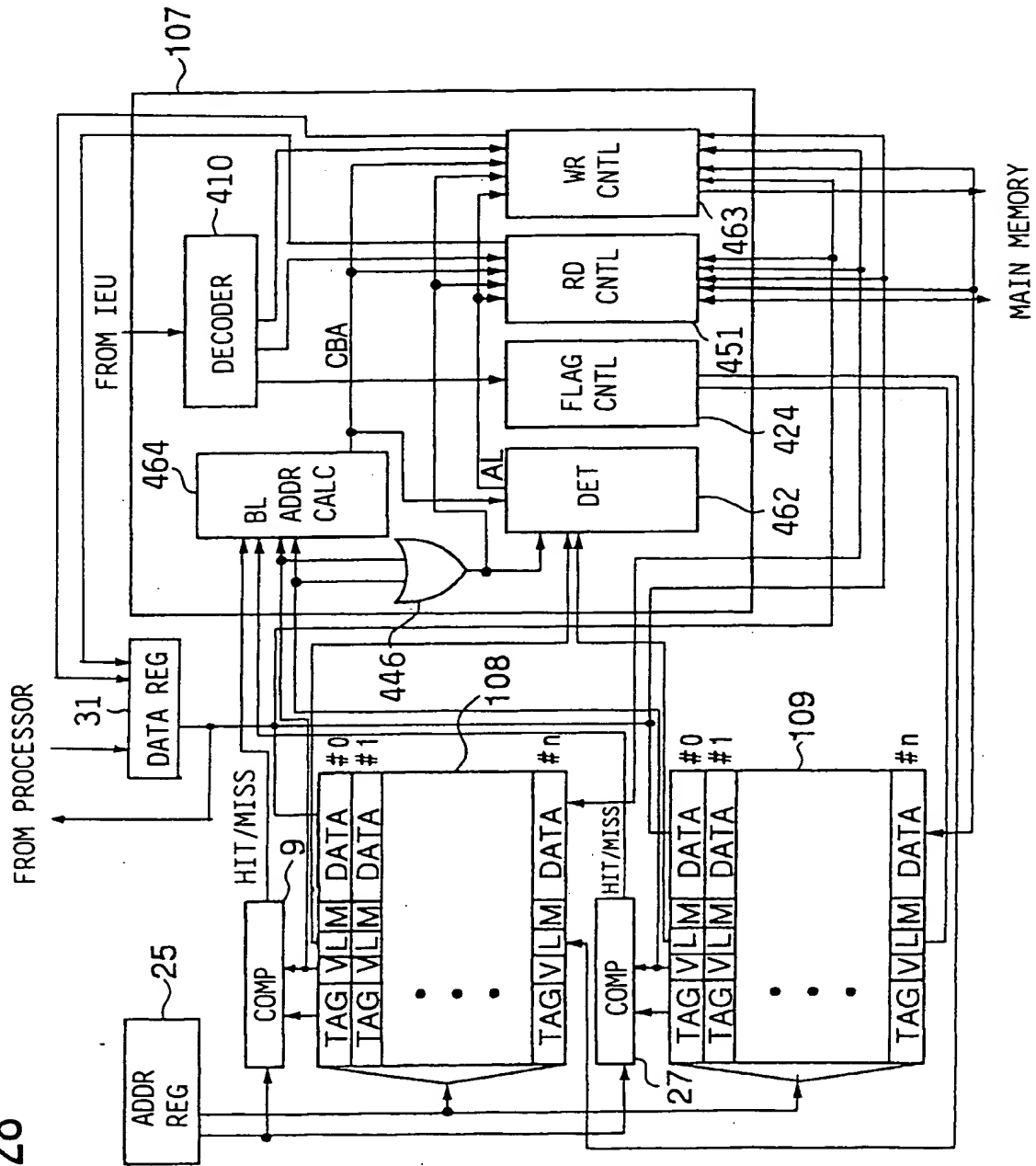


FIG. 29

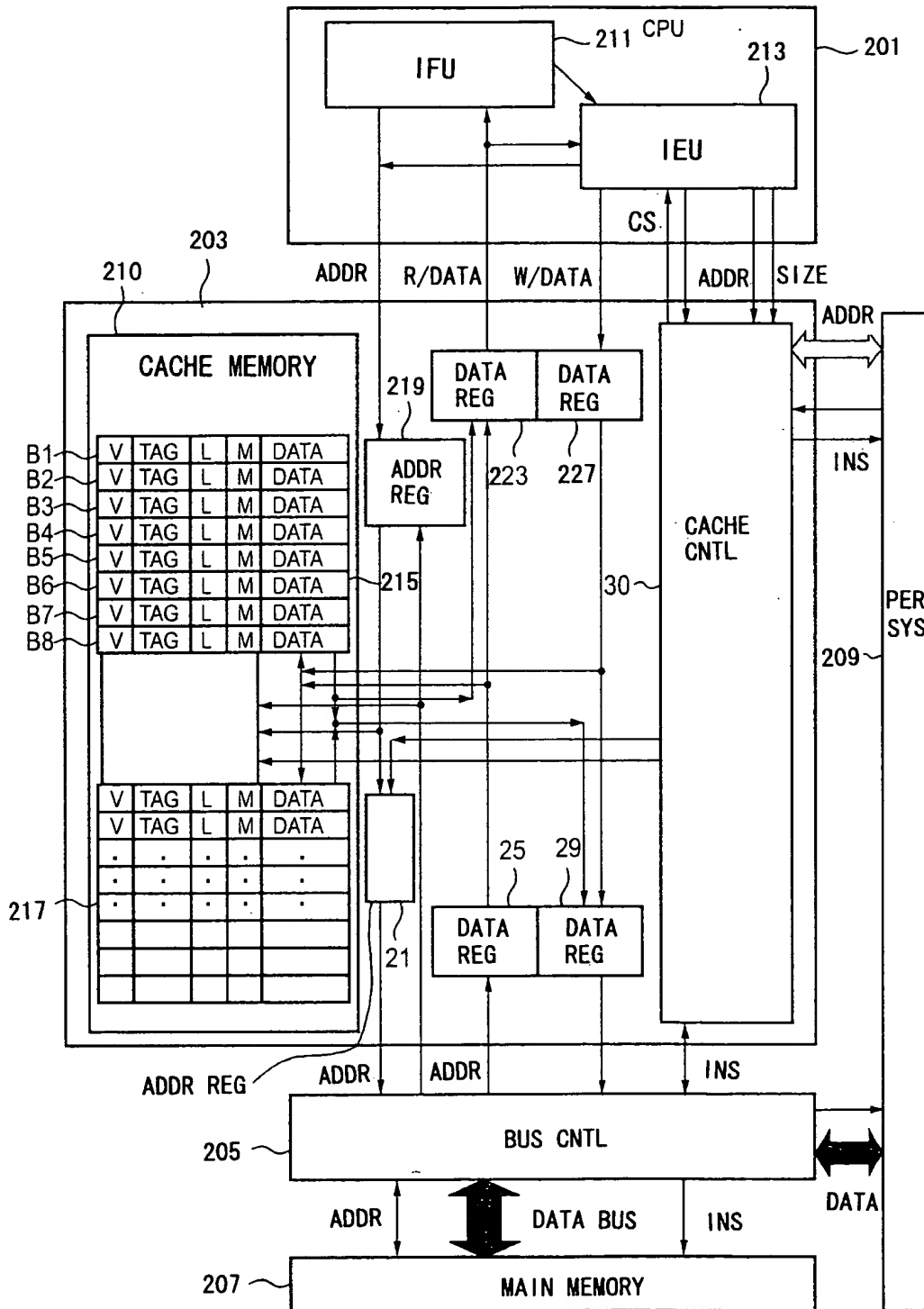
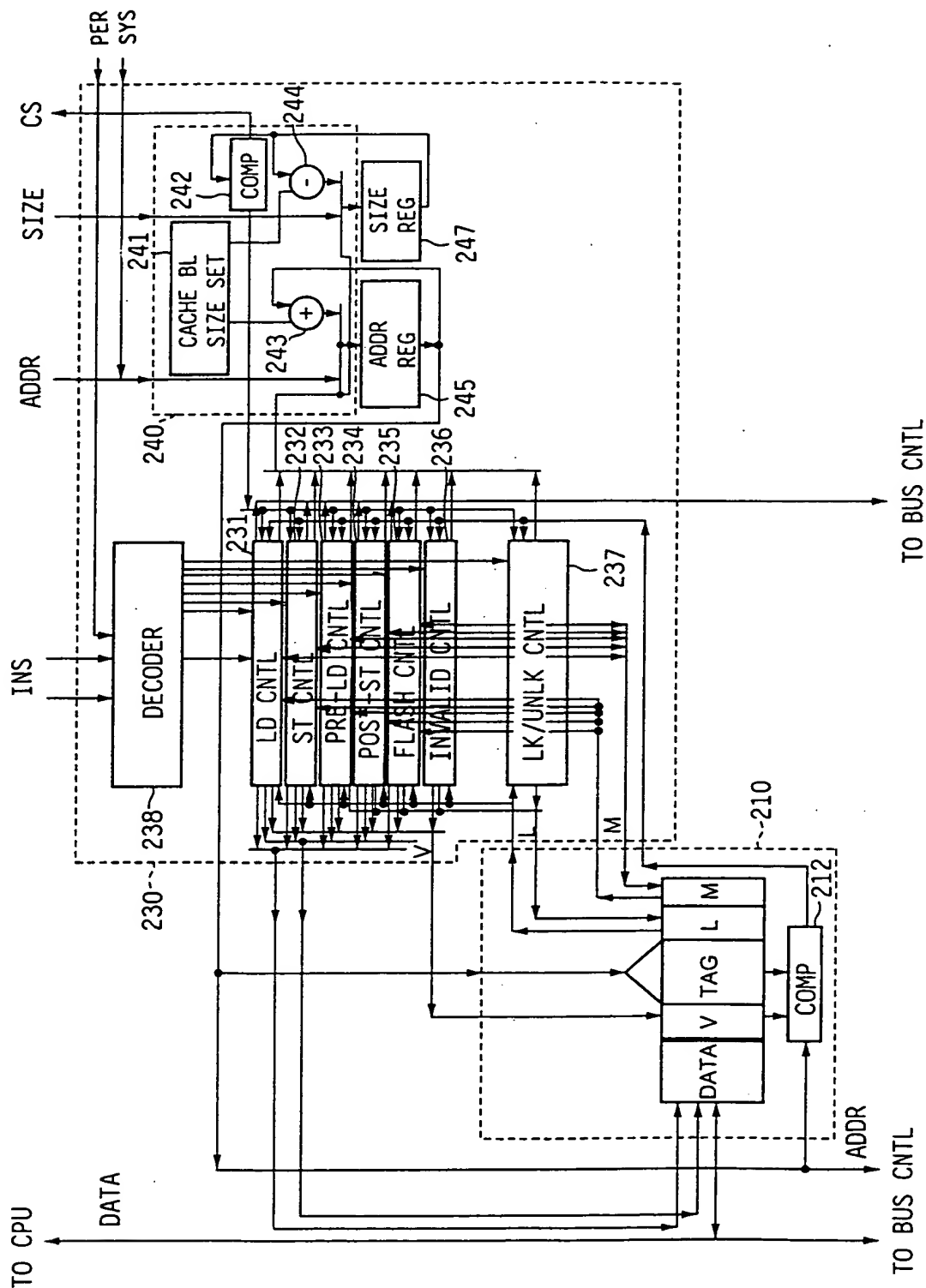


FIG. 30



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FIG. 31

OP-CODE	AD	SIZE
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FIG. 32

OP-CODE	AD	SIZE	LOCK
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APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

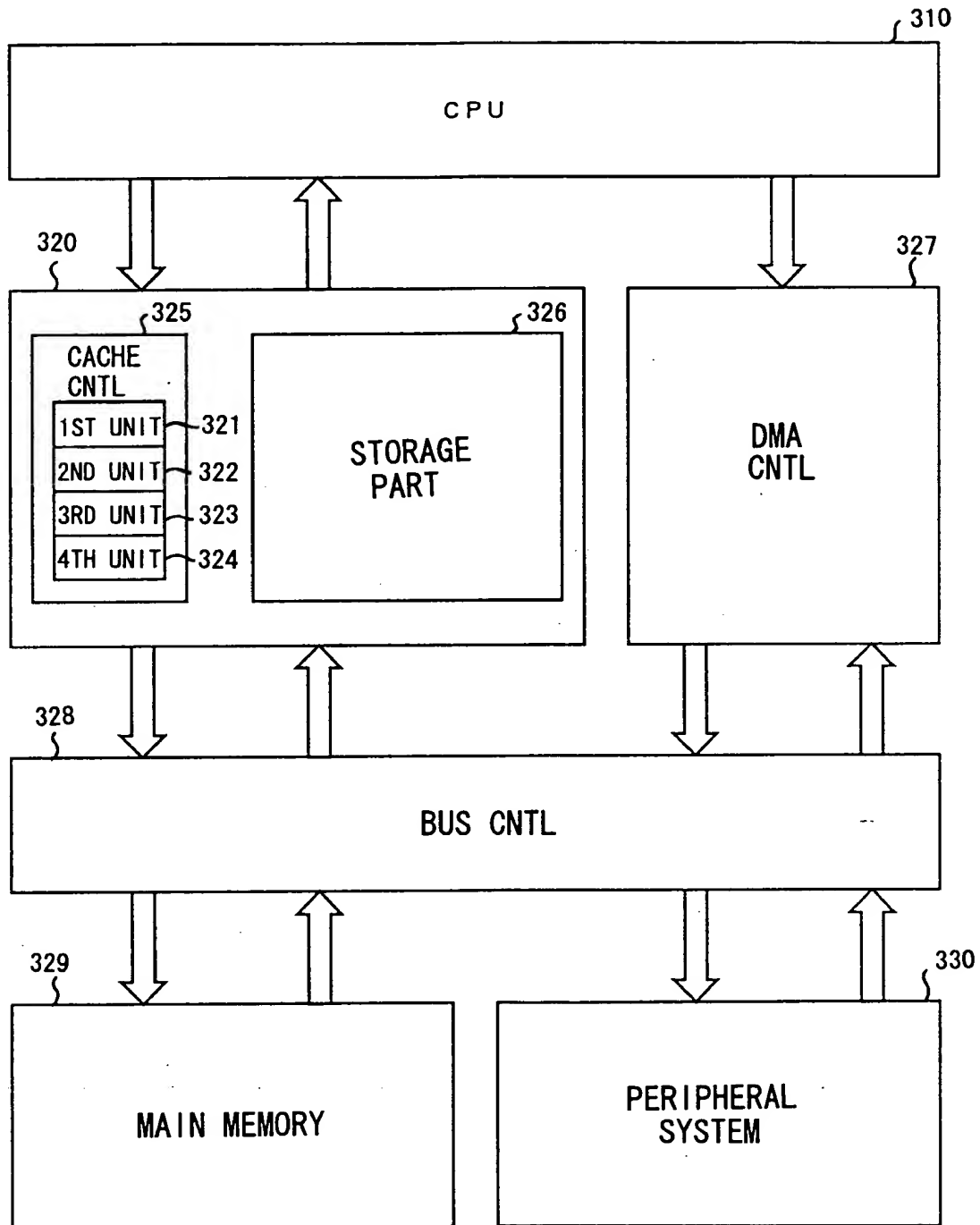
FIG. 33

OP-CODE	AD	SIZE	FORCE
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FIG. 34

OP-CODE	AD	REG
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FIG. 35



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FIG. 36

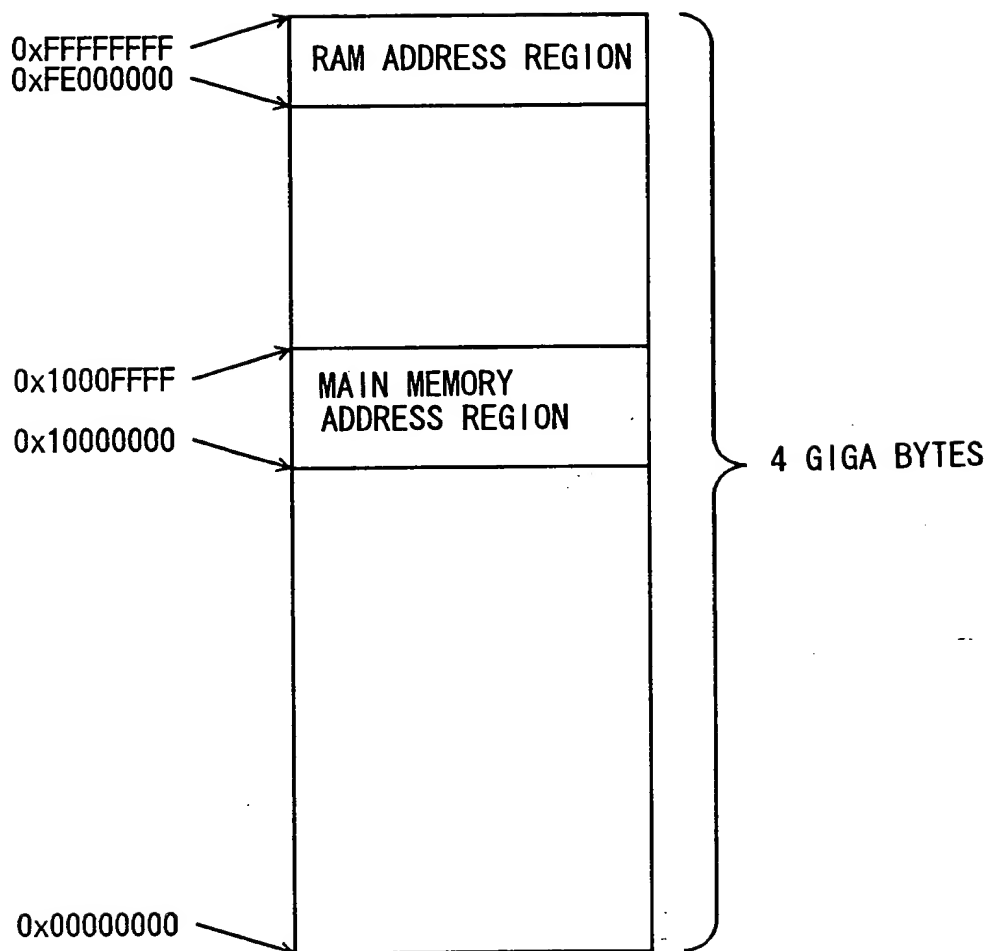


FIG. 37

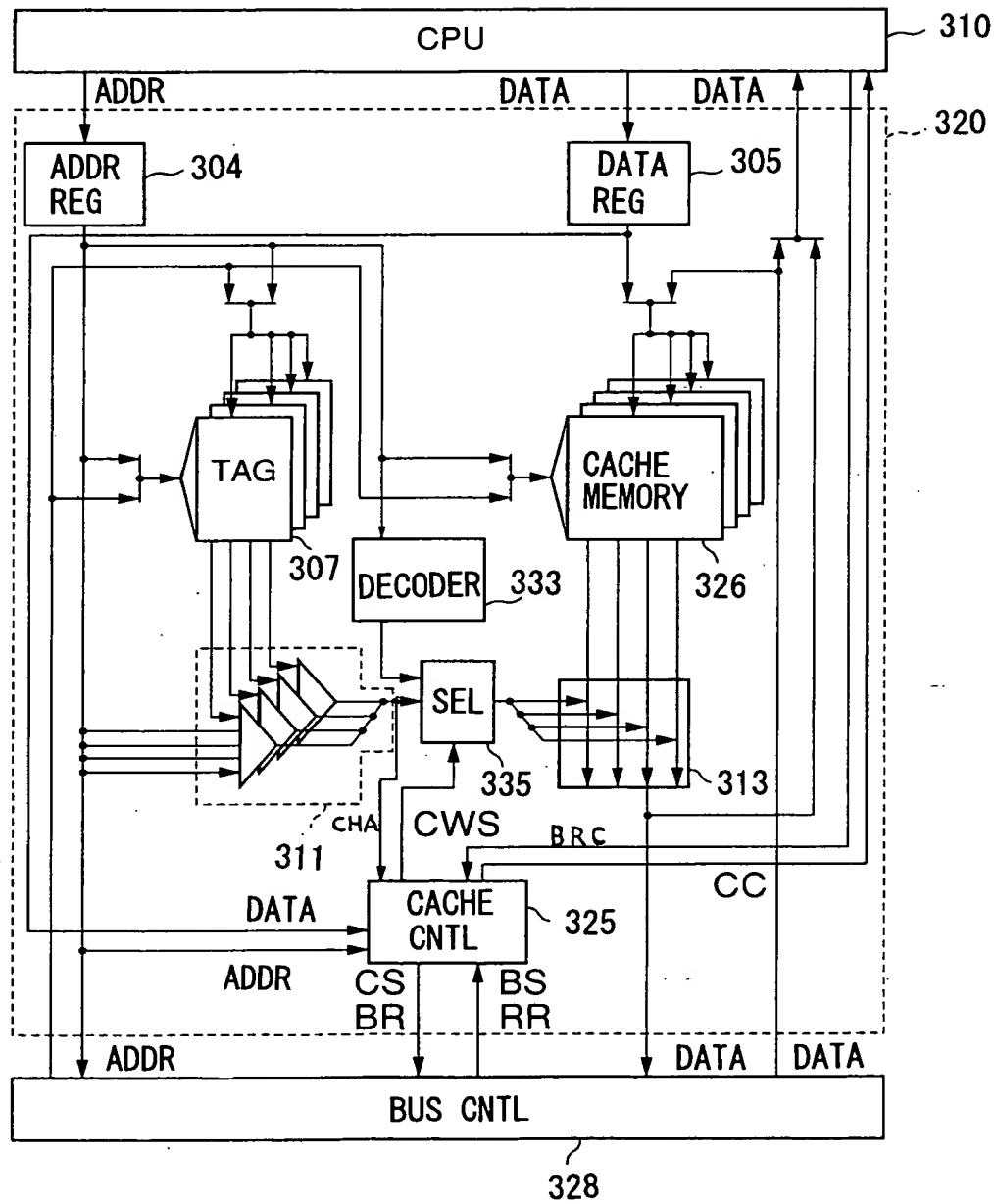


FIG. 38

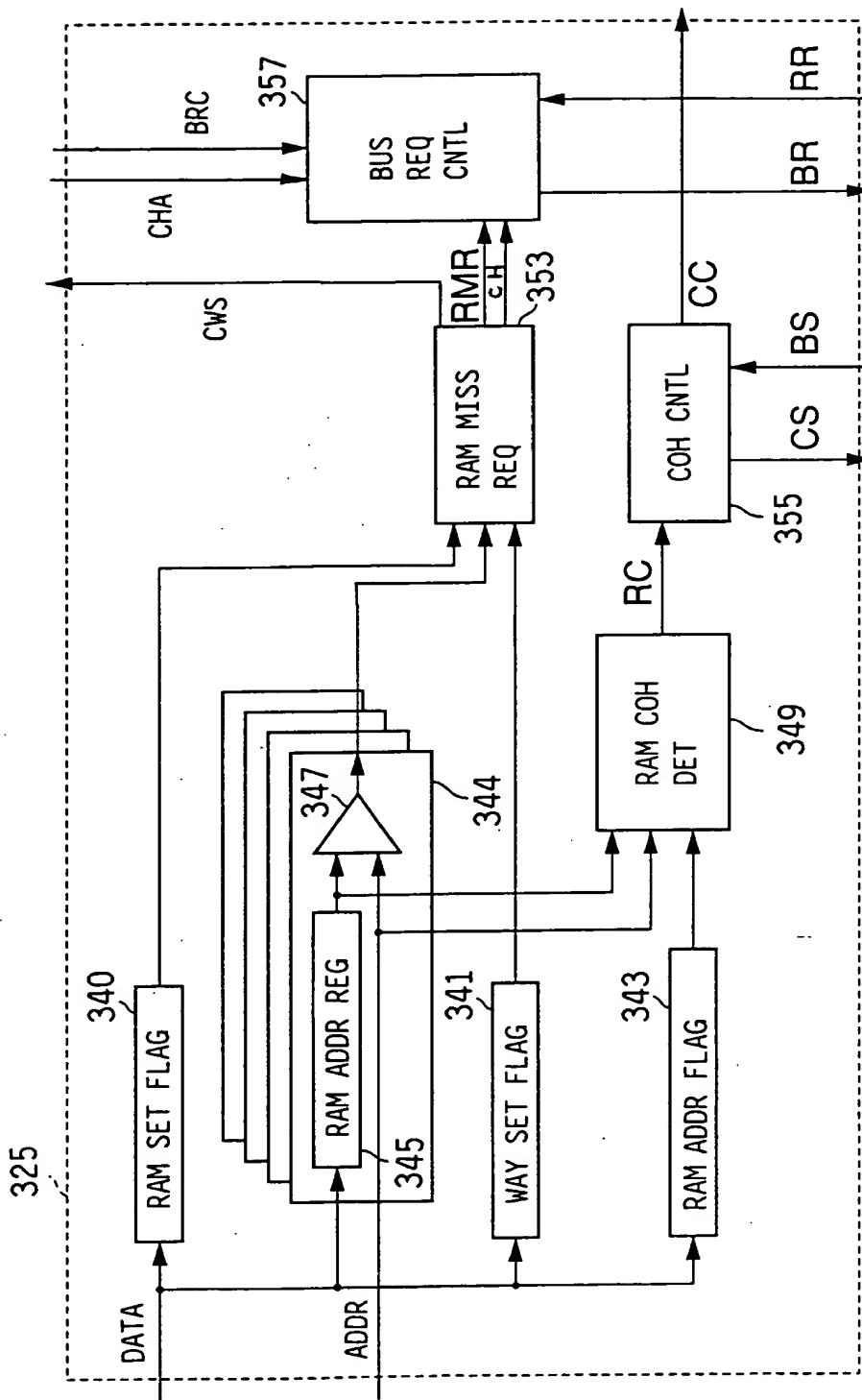


FIG. 39

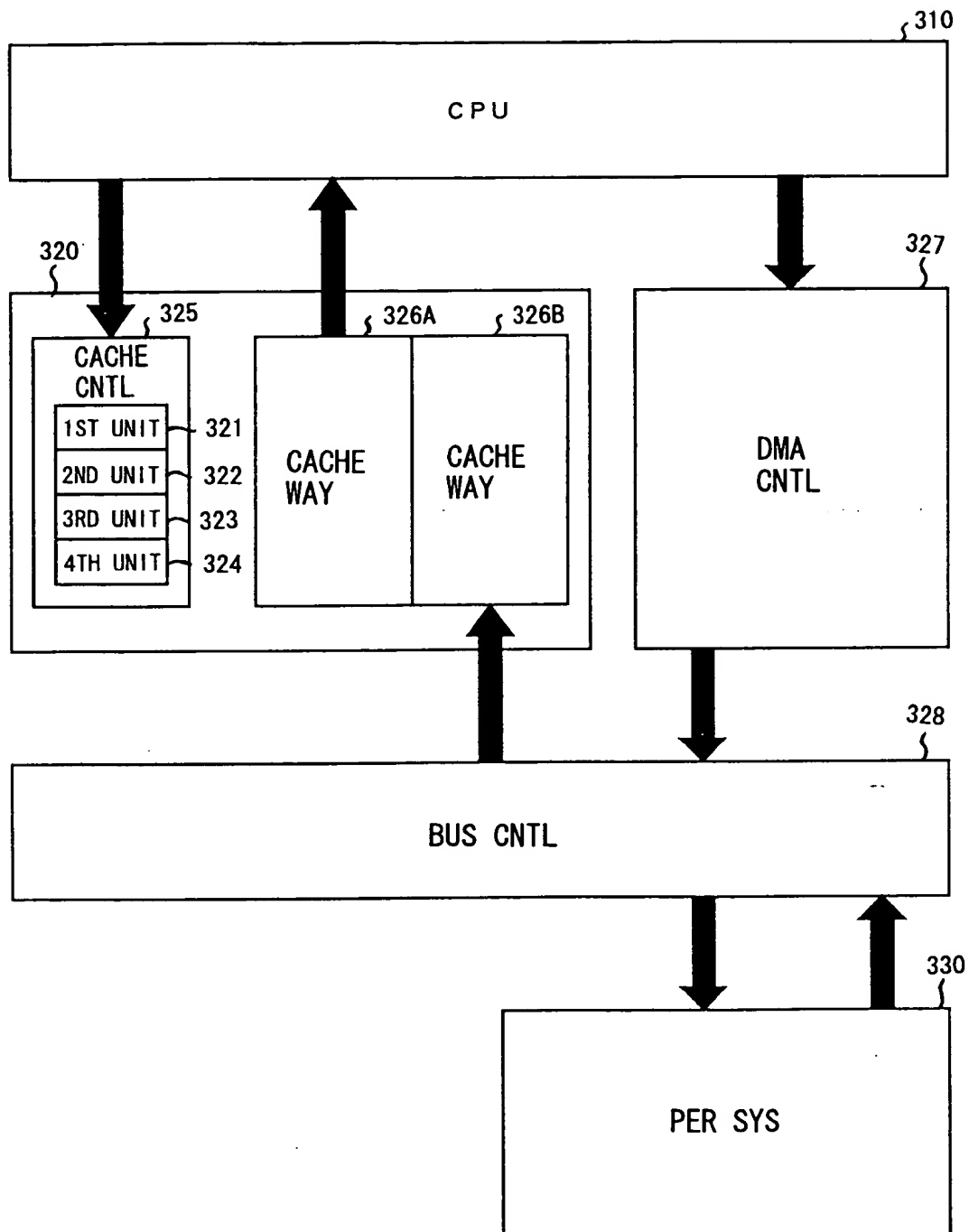


FIG. 40

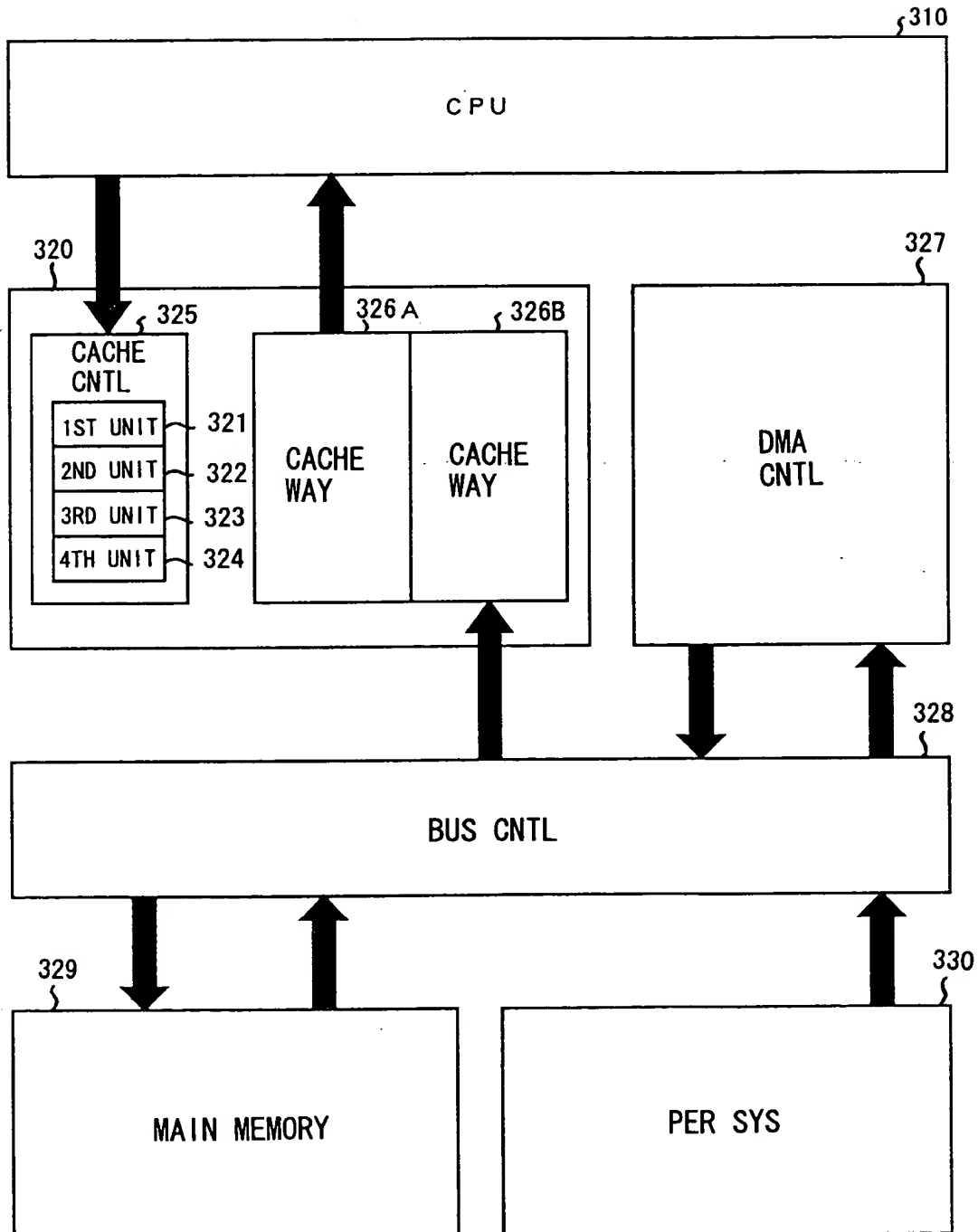


FIG. 41

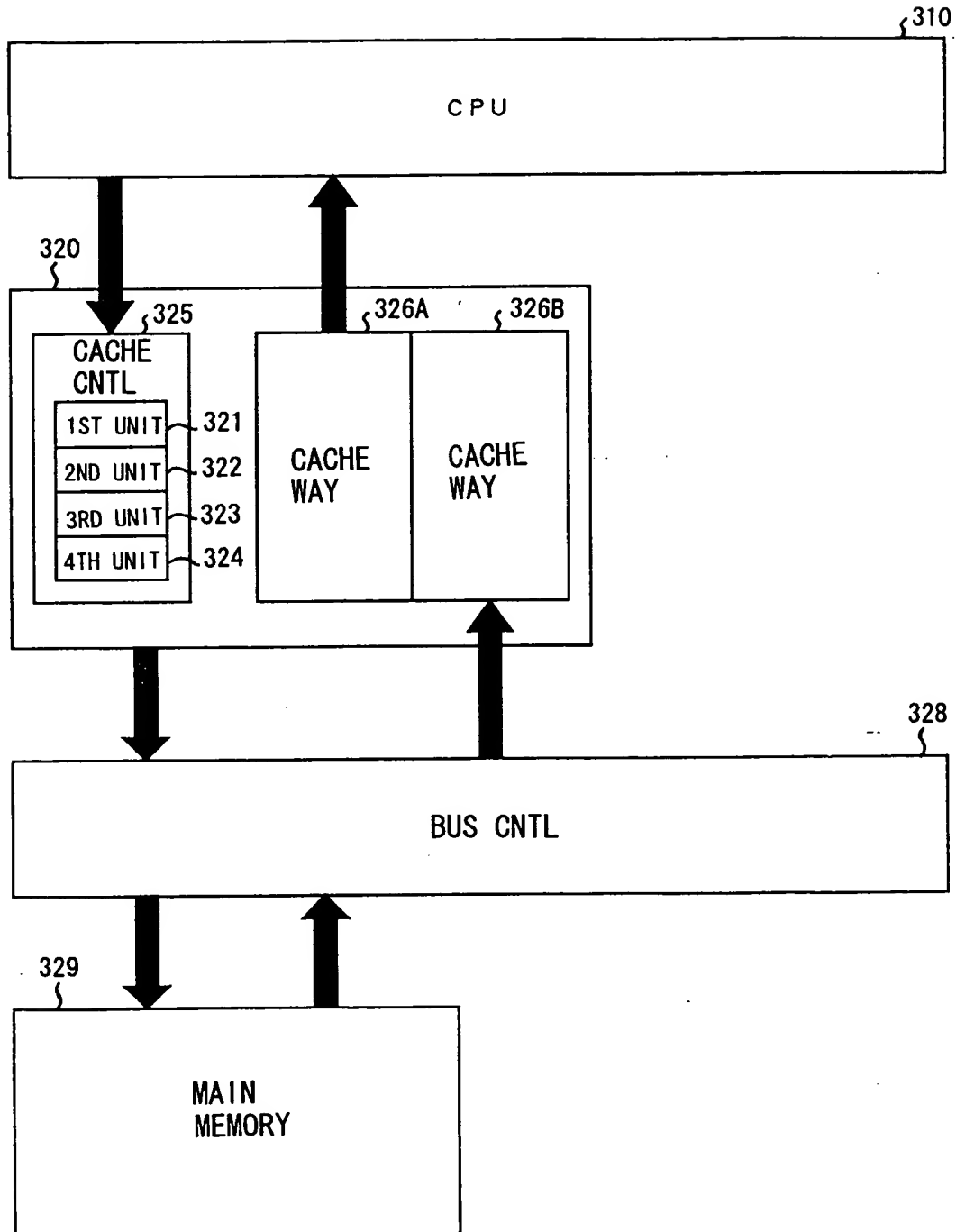


FIG. 42

